Memory Short Course Program
Embedded Memory Design

Honolulu I
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs:	John Barth, IBM Masao Ito, Renesas Technology Corporation
8:10 a.m.	**Introduction** J. Barth, IBM
8:15 a.m.	**Embedded Memory Overview (and DRAM)** S. Natarajan, TSMC Design Technology Canada
9:25 a.m.	**Static RAM** M. Yamaoka, Hitachi, Ltd.
10:35 a.m.	**Break**
10:50 a.m.	**Floating Body RAM** T. Ohsawa, Toshiba Corporation
12:00 p.m.	**Lunch**
1:30 p.m.	**Phase Change RAM** C. Lam, IBM
2:40 p.m.	**Break**
2:55 p.m.	**Flash** R. Kakoschke, Infineon
4:05 p.m.	**Built in Self Test** D. Weiss, AMD
5:15 p.m.	**Conclusion** M. Ito, Renesas Technology Corporation

(See next page for Analog Digital Short Course schedule)

Analog/Digital Short Course Program
Embedded Power Management Circuits and Systems

Honolulu II
Tuesday, June 17, 8:10 a.m.

Organizers/Chairs: Tom Kwan, Broadcom Corporation
Koichi Nose, NEC Corporation

8:10 a.m. **Introduction**
T. Kwan, Broadcom Corporation

8:15 a.m. **Overview of Embedded Power Management Circuits and Systems in SoC's**
D. Anderson, National Semiconductor Corp.

9:25 a.m. **Integrated Power Management for Mobile SoC's**
D. Ho, Broadcom Corporation

10:35 a.m. **Break**

10:50 a.m. **Circuit Design for Power Management Building Blocks**
W.-H. Ki, Hong Kong University of Science and Technology

12:00 p.m. **Lunch**

1:30 p.m. **Thermal Management of High-Performance Processors**
E. Miranda, Analog Devices Corp.

2:40 p.m. **Break**

2:55 p.m. **Power Management at the System/Architecture/Circuit Level**
M. Nomura, NEC

4:05 p.m. **Dynamic Power/Thermal Management in High Performance Processors; Examples and Opportunities**
S. Naffziger, AMD

5:15 p.m. **Speaker Interview Session**