SESSION 14 – TAPA I
Trapped Charge NVM

Thursday, June 19, 8:30 a.m.
Chairpersons: K.-M. Chang, Freescale Semiconductor
J. Lee, MagnaChip Semiconductor Ltd.

14.1 - 8:30 a.m.

Embedded Split-Gate Flash Memory with Silicon Nanocrystals for 90nm and Beyond, G. Chindalore, J. Yater, H. Gasquet, M. Suhail, S.-T. Kang, C.M. Hong, N. Ellis, G. Rinkenberger, J. Shen, M. Herrick, W. Malloch, R. Syzdek, K. Baker, K.-M. Chang, Freescale Semiconductor, USA

We present a split-gate based NOR flash memory array with silicon nanocrystals as the storage medium. 128KB memory arrays have been evaluated with this technology and the results presented here show a nanocrystal memory that has been demonstrated to achieve a minimum 1.5B operating window that is maintained through 10K program/erase cycles; well controlled array threshold distributions; fast source-side injection programming (10-20us); fast tunnel erase into the gate; and robust high temperature data retention for both uncycled and cycled arrays. Results presented here with focus on the array operation demonstrate the maturity of this technology for implementation into consumer, industrial, and automotive microcontrollers.

14.2 - 8:55 a.m.

Gate-all-around Single Silicon Nanowire MOSFET with 7 nm Width for SONOS NAND Flash Memory, K.H. Yeo, K.H. Cho, M. Li, S.D. Suk, Y.-Y. Yeoh, M.-S. Kim, H. Bae, J.-M. Lee, S.-K. Sung, J. Seo, B. Park, D.-W. Kim, D. Park, W.-S. Lee, Samsung Electronics Co., Korea

Gate-all-around (GAA) MOSFET with single silicon nanowire is fabricated and applied to SONOS memory as a cell transistor for NAND flash string. Driving current over 1uA, which is sufficient to NAND string, is obtained with single nanowire of ~7 nm width. Using FN tunneling conditions, VTH window of 4.5V and fast program/erase (P/E) speed of ~10us are obtained, respectively. The smaller nanowire width is, the faster program speed and the larger VTH shift are achieved. P/E operations in NAND string with GAA SONOS nanowire are demonstrated for the first time.

14.3 - 9:20 a.m.

A Novel Junction-Free BE-SONOS NAND Flash, H.-T. Lue, E.-K. Lai, Y.H. Hsiao, S.P. Hong, M.T. Wu, F.H. Hsu, N.Z. Lien, S.Y. Wang, L.W. Yang, T. Yang, K.C. Chen, K.Y. Hsieh, R. Liu, C.-Y. Lu, Macronix International Co., Taiwan

We have successfully demonstrated a novel junction-free BE-SONOS NAND Flash. Junction-free devices greatly improve the short channel effect and thus promise scaling of NAND Flash below 20nm node. Instead of S/D junctions a very small space (< 30nm) is left between adjacent devices. Junction is formed only at the outer region of NAND array, while there is no junction inside the array. Successful n-channel, p-channel and TFT BE-SONOS NAND devices are demonstrated using this technique. This new device can be implemented in the current NAND Flash process without introducing new masks.

14.4 - 9:45 a.m.

Enhanced Endurance of Dual-bit SONOS NVM Cells Using the GIDL Read Method, A. Padilla, S. Lee, D. Carlton, T.-J. King Liu, University of California at Berkeley, USA

Gate-induced drain leakage (GIDL) current is demonstrated to be more sensitive to charge stored locally within the gate-dielectric stack, as compared with the transistor threshold voltage (VT). Thus the sensing of GIDL rather than VT is advantageous for dual-bit SONOS NVM cell read operation, not only because it mitigates the complementary-bit disturb (CBD) issue and hence facilitates gate-length scaling, but also because it allows for reductions in stored charge and hence lower program/erase voltages for improved endurance.