SESSION 16 – TAPA I
Variation

Thursday, June 19, 10:25 a.m.
Chairpersons: M.-R. Lin, AMD
T. Hiramoto, University of Tokyo

16.1 - 10:25 a.m.

Analyses of 5σ Vth Fluctuation in 65nm-MOSFETs Using Takeuchi Plot, T. Tsunomura, A. Nishida, F. Yano, A.T. Putra**, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada*, T. Hiramoto, T. Mogami, MIRAI-Selete, *Hiroshima City University, **University of Tokyo, Japan

Using 1M DMA-TEG, the analyses of 5σ Vth fluctuation in 65nm-MOSFETs were carried out. Physical and electrical analyses confirmed that random dopant fluctuation is dominant though NMOSFET has larger fluctuation as compared with PMOSFET. To explain this phenomenon, a B clustering model is proposed. In the case of clustering with 5 to 6 B atoms in the channel, Vth fluctuation of NMOSFET can be explained.

16.2 - 10:50 a.m.

Reduction of Vth Variation by Work Function Optimization for 45-nm Node SRAM Cell, G. Tsutsui, K. Tsunoda, N. Kariya, Y. Akiyama, T. Abe, S. Maruyama, T. Fukase, M. Suzuki, Y. Yamagata, K. Imai, NEC Electronics Corporation, Japan

Work function (WF) control is a key technology that can reduce channel impurity resulting in the decrease in intrinsic random dopant variation (IRDV). It is demonstrated that saturation Vth is affected not only by IRDV but also by S factor variation owing to fluctuation of DIBL. While channel impurity reduction by WF control decreases IRDV, DIBL is degraded in turn, and this enhances S factor variation. The optimal VFB shift by WF control is determined by two competing factors, S factor variation and IRDV. With this technique Vth variation of 45-nm SRAM comparable to 65-nm, despite cell size reduction is obtained.

16.3 - 11:15 a.m.

45nm Low-Power CMOS SoC Technology with Aggressive Reduction of Random Variation for SRAM and Analog Transistors, S. Ekbote, K. Benaissa, B. Obradovic, S. Liu, H. Shichijo, F. Hou, T. Blythe, T. Houston, S. Martin, R. Taylor, A. Singh, H. Yang, G. Baldwin, Texas Instruments, USA

Mobile System-on-Chip technologies require high-quality analog components, low-power CMOS and dense SRAM. However, area scaling for both the SRAM bit cell and analog CMOS circuits is becoming increasingly difficult due to the impact of transistor random variation. To avoid added cost, co-optimizing the process for low random variation along with high performance and low power is required. We report a 45nm low-power technology with significantly reduced random variation for high yielding 0.255µm2 SRAM arrays and analog transistors. Flexible RF and passive components for mobile SoC's are also described. These process techniques enable continued 50% area scaling at 45nm and beyond.

16.4 - 11:40 a.m.

Understanding and Prediction of EWF Modulation Induced by Various Dopants in the Gate Stack for a Gate-First Integration Scheme, X.P. Wang, H.Y. Yu, Y.-C. Yeo*, M.-F. Li*^^, S.-Z. Chang**, H.-J. Cho^, S. Kubicek, D. Wouters, G. Groeseneken, S. Biesemans, IMEC, Belgium, *National University of Singapore, Singapore, **TSMC, ^Samsung, Taiwan, ^^Fudan University, China

For the first time, after considering the thermodynamic properties (evaluated by the molar Gibbs energy of oxide formation, $\Delta_{Oxide}G$) and the electronegativity (x), a practical model to understand the EWF modulation induced by the various dopants is proposed. It is found that the dopant oxide will determine the EWF if the $\Delta_{Oxide}G$ of dopant is more negative than that of host gate oxide. Or else, x difference between dopants and host materials will play a more critical role for determining the EWF. This model can serve as a guideline for understanding the EWF modulation by various dopants and to select the appropriate gate stack materials for the gate-first technology.