SESSION 17 – HONOLULU SUITE
Advanced SOI

Thursday, June 19, 10:25 a.m.
Chairpersons: T. Skotnicki, STMicroelectronics
T. Wakabayashi, Sony Corporation

17.1 - 10:25 a.m.
Smallest V_{th} Variability Achieved by Intrinsic Silicon on Thin BOX (SOTB) CMOS with Single Metal Gate, Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu*, T. Ipposhi*, H. Oda*, Y. Inoue*, K. Torii, S. Kimura, Hitachi Ltd., *Renesas Technology Corp., Japan

"Silicon on thin BOX" (SOTB) achieved the smallest Vth variability. The Pelgrom coefficients were 1.8 (NMOS) and 1.5 (PMOS), even in the case of relatively thick EOT of 1.9 nm. In this SOTB, multi-Vth control and suppression of short-channel effects were performed by adjusting the impurity concentration beneath the BOX keeping the channel almost intrinsic. pd and Ioff were optimized by controlling gate-overlap using a dual-layer offset spacer. The scalability of the SOTB is shown.

17.2 - 10:50 a.m.
Selenium Co-implantation and Segregation as a New Contact Technology for Nanoscale SOI N-FETs Featuring NiSi:C Formed on Silicon-Carbon (Si:C) Source/Drain Stressors, H.-S. Wong, F.-Y. Liu, K.-W. Ang*, S.-M. Koh, A.T.-Y. Koh, T.-Y. Liow, R.T.-P. Lee, A.E.-J. Lim, W.-W. Fang, M. Zhu, L. Chan, N. Balasubramaniam*, G. Samudra, Y.-C. Yeo, National University of Singapore, *Institute of Microelectronics, Singapore

We report a novel contact technology comprising Selenium (Se) co-implantation and segregation to reduce Schottky barrier height ΦBn and contact resistance for n-FETs. Introducing Se at the silicide-semiconductor interface pins the Fermi level near the conduction band, and achieves a record low ΦBn of 0.1 eV on Si:C S/D stressors. Comparable sheet resistance and junction leakage are observed with and without Se segregation. When integrated in nanoscale SOI n-FETs with Ni-silicided Si:C S/D, the new Se-segregation contact technology achieves 36% reduction in total series resistance and 32% ION enhancement. Linear transconductance GML in also shows large enhancement in the sample with Se-segregated contacts.

17.3 - 11:15 a.m.
Mobility Of Strained And Unstrained Short Channel FD-SOI Mosfets: New Insight By Magnetoresistance, M. Casse, F. Rochette, N. Bhouri, F. Andrieu, D.K. Maude*, M. Mouis**, G. Reimbold, F. Boulanger, CEA-LETI MINATEC, *CNRS-GHMFL, **IMEP CNRS/INPG/UJF, France

Electron mobility in strained and unstrained FD-SOI MOSFETs is deeply investigated in linear regime by careful magnetoresistance measurements down to 40nm gate length and 20K. This method differs from standard ones because: it does not require any data on the short channel gate capacitance and gate length; it is more accurate at low inversion charge; the temperature dependence of the Coulomb Scattering (CS) limited mobility is higher. Additional mobility scattering has been confirmed for short channel nMOS, and unambiguously identified as CS. A 50% mobility gain for strained Si MOSFETs is still observable even in this dominant CS regime.

17.4 - 11:40 a.m.
On Implementation of Embedded Phosphorus-doped SiC Stressors in SOI nMOSFETs, Z. Ren, G. Pei*, J. Li, B.F. Yang*, R. Takalkar, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, J. Miller, A. Dube, L. Black*, J.W. Weijtmans*, B. Yang*, E. Harley, A. Chakravarti, T. Kanarsky, R. Pal*, I. Lauer^, D.-G. Park^, D. Sadana^, IBM SRDC, ^IBM T.J. Watson Research Center, *AMD Inc., USA

We report a successful implementation of epitaxially grown Phosphorus-doped (P-doped) embedded SiC stressors into SOI nMOSFETs. We identify a process integration scheme that best preserves the SiC strain and minimizes parasitic resistance. At a substitutional C concentration (Csub) of ~1.0%, high performance nFETs with SiC stressors demonstrate ~9% enhanced Ieff and ~15% improved Idlin against the well calibrated control devices. It is found that the tensile liner technique provides further performance improvement for nFETs with SiC stressors, whereas the Stress Memory Technique (SMT) does not provide performance gain in a laser annealing process that is used to preserve SiC strain. The material quality of the SiC stressors strongly affects strain transfer.