SESSION 18 – TAPA I
Performance Enhanced CMOS

Thursday, June 19, 1:30 p.m.
Chairpersons: K. Schruefer, Infineon Technologies
H. Kurata, Fujitsu Laboratories Ltd.

18.1 - 1:30 p.m.
A Designer Friendly 45nm High Performance Technology with In-situ C-doped e-SiGe & Dual Stress Liner in SRAM, R. Khamankar, C. Bowen, H. Bu, D. Corum, I. Fujii, B. Hornung, T. Kim, B. Kirkpatrick, K. Kirmse, A. Krishnan, C. Lin, L. Liu, T. Lowry, C. Montgomery, O. Olubuyide, S. Prins, D. Riley, S. Yu, J. Blatchford, C. Machala, C. O'Brien, G. Shin, T. Grider, Texas Instruments, USA

A 45nm high performance technology with 11 level metallization is presented for SOC applications. High performance and density are maintained through new process optimizations that allow the use of less restrictive layouts by eliminating defect generation from strain enhancing processes. Additionally, technology modeling has been made simpler through optimization of key processes to minimize context dependences while simultaneously providing a competitive technology. High drive currents of 1150uA/um and 720uA/um are obtained for nMOS and pMOS, respectively at 1.0V and Ioff of 100nA/µm. The first yielding SRAMs incorporating both in-situ C-doped e-SiGe and dual stress liner (DSL) in SRAM are demonstrated.

18.2 - 1:55 p.m.
Higher Hole Mobility Induced By Twisted Direct Silicon Bonding (DSB), M. Hamaguchi, H. Yin*, K. Saenger**, C.-Y. Sung**, R. Hasumi, R. Iijima, K. Ohuchi, Y. Takasu, J. Ott**, H. Kang*, M. Biscardi*, J. Li*, A. Domenicucci*, Z. Zhu*, P. Ronsheim*, R. Zhang*, N. Rovedo*, H. Utomo*, K. Fogel**, J.P. De Souza**, D.K. Sadana**, M. Takayanagi, D. Park*, G. Shahidi*, K. Ishimaru, Toshiba America Electronic Components Inc., *IBM SRDC, **IBM T.J. Watson Research Center, USA

Twisted Direct Silicon Bonded (DSB) substrate demonstrates a higher hole mobility advantage over (110) bulk substrate for PFET. The mobility shows a (110) layer thickness dependence with the thinner DSB layer having a higher hole mobility. Moreover, the thinner DSB shows better short channel characteristics. Twisted thin DSB substrate demonstrates 11% faster ring oscillator speed over thick DSB substrate and 30% faster over (100) bulk due to higher mobility and lower capacitance.

18.3 - 2:20 p.m.
32nm Device Architecture Optimization for Critical Path Speed Improvement, R. Gwoziecki, S. Kohler, F. Arnaud, STMicroelectronics, France

This study investigates key elements improving CMOS critical path speed. We proposed a full analysis of input signal slope impact on the switching current trajectories depending on Vt centering. Based on inverter output characteristics shape, we demonstrated that speed of low-Vt (LVT) path preferred higher drive current (ION) whereas high-Vt (HVT) cells speed is enhanced by lower Drain Induced Barrier Lowering (DIBL). Finally, we proposed a link with transistor architecture by optimizing halos and Light-Doping-Drain (LDD) design to improve logic gate as a function of Vt options.

18.4 - 2:45 p.m.
Strain Additivity in III-V Channels for CMOSFETs Beyond 22nm Technology Node, S. Suthram, Y. Sun^, P. Majhi, I. Ok*, H. Kim*, H.R. Harris, N. Geol, S. Parthasarathy^, A. Koehler^, T. Acosta^, T. Nishida^, H.-H. Tseng, W. Tsai**, J. Lee*, R. Jammy, S.E. Thompson^, SEMATECH, *University of Texas at Austin, **Intel Corp., ^University of Florida, USA

For the first time strain additivity on III-V using prototypical (100) GaAs n- and p-MOSFETs is studied via wafer bending experiments and piezoresistance coefficients are extracted and compared with those for Si and Ge MOSFETs. Further understanding of these results is obtained by using multi-valley conduction band model for n-MOS and performing k.p simulations for p-MOS. For GaAs n-MOSFET, uniaxial tensile stress is shown to enhance performance only for small stresses biaxial tensile stress is shown to be more beneficial. Importantly uniaxial compressive stress is beneficial for GaAs pMOSFETs and the piezoresistance effect is much larger than that seen for Si MOSFETs along the <110> channel direction.