SESSION 19 – HONOLULU SUITE
**Advanced Junction Technology II**

Thursday, June 19, 1:30 p.m.
Chairpersons: F. Nouri, Applied Materials, Inc.
E. Morifuji, Toshiba Corp. Semiconductor Co.

**19.1 - 1:30 p.m.**
**Laser-Annealed Junctions with Advanced CMOS Gate Stacks for 32nm Node: Perspectives on Device Performance and Manufacturability,** C. Ortolland, T. Noda, T. Chiarella, S. Kubicek, C. Kerner, W. Vandervorst, A. Opdebeeck, C. Vrancken, N. Horiguchi, M. De Potter, M. Aoulaiche, E. Rosseel, S. Felch*, P. Absil, R. Schreutelkamp*, S. Biesemans, T. Hoffmann, IMEC, Belgium, *Applied Materials, USA

We report on the integration of laser-annealed junctions into a state-of-the-art high-k/metal gate process flow. We achieve excellent Lg scaling of 15/30nm over a Spike reference, for nMOS and pMOS respectively, without any performance loss. This enables to fabricate transistors with Lgmin meeting the 32nm node requirement. In addition, we highlight the implication of MG integration flow on the junctions design. Also, we demonstrate that MSA only process can fulfill even the stringent junction leakage requirement for LP applications. Finally we show for the very first time that micro-uniformities specific to this diffusion-less process have a negligible electrical impact.

**19.2 - 1:55 p.m.**
**Advanced Junction Profile Design Scheme by Low-temperature Millisecond Annealing and Co-implant for High Performance CMOS,** K. Ikeda, T. Miyashita, T. Kubo*, T. Yamamoto, T. Sukegawa*, K. Okabe*, H. Ohta, Y.S. Kim, H. Nagai*, M. Nishikawa*, Y. Shimamune, A. Hatada*, Y. Hayami, K. Ohkoshi*, N. Tamura, K. Sukegawa, H. Kurata, S. Satoh, M. Kase*, T. Sugii, Fujitsu Laboratories Ltd., *Fujitsu Limited, Japan

We found that the relatively low temperature millisecond annealing at S/D activation for nFET is enhanced the co-implanted halo activation regardless of sequence of MSA and spike-RTA. Tilt-and-twist extension implantation technique with millisecond extension annealing for pFET was also performed to reduce the parasitic resistance. By combining these technique, an aggressively scaled high-performance bulk CMOS transistors with world competitive nFET and pFET drive currents of 1282/835μA/μm at 100nA/um off-current at Vd=1V and Lg=34nm respectively, were developed with conventional poly/SiON gate stack. The developed CMOS transistors not only have high-performance but also manufacturing friendly and cost-effective compared with metal/high-k stack devices.

**19.3 - 2:20 p.m.**
**Low $V_t$ Gate-First Al/TaN/[$Ir_3Si$-$HfSi_{2-x}$]/HfLaON CMOS Using Simple Laser Annealing/Reflection,** C.C. Liao, A. Chin, N.C. Su*, M.-F. Li**, S.J. Wang*, National Chiao-Tung University, *National Cheng Kung University, Taiwan, **National University of Singapore, Singapore

We report low Vt Al/TaN/[Ir3Si-HfSi2-x]/HfLaON CMOS using simple laser annealing/reflection with self-aligned and gate-first process compatible with current VLSI. At 1.05 nm EOT, good effective work-function of 5.04 and 4.24 eV, low Vt of -0.16 and 0.13 V, high mobility of 85 and 209 cm2/Vs, and small 85oC BTI<=40 mV (10 MV/cm, 1 hr) are measured for p- and n-MOSFETs. This good device integrity was achieved using laser annealing on ion-implanted source-drain and simultaneously high laser reflection by Al-covered gate electrode with lower thermal budget under the gate and less VFB roll-off.

**19.4 - 2:45 p.m.**
**Successful Enhancement of Metal Segregation at NiSi/Si Junction through Pre-amorphization Technique,** Y. Nishi, Y. Tsuchiya, A. Kinoshita, A. Hokazono, J. Koga, Toshiba Corporation, Japan

A new technique to enhance the metal segregation at NiSi/Si interface for reducing contact resistance in source/drain electrodes is proposed. It is demonstrated that metal segregation at the junction of pre-amorphized NiSi/Si using ion-implantation leads to reduction of Schottky barrier height by >0.2eV. This modulation width is far beyond the previous metal segregation technique and allows 90% reduction of contact resistance in source/drain junctions for further scaling of MOSFETs.