SESSION 20 – TAPA I
CMOS Imager and Novel Memory

Thursday, June 19, 3:25 p.m.
Chairpersons: F. Nouri, Applied Materials Inc.
H. Wakabayashi, Sony Corporation

20.1 - 3:25 p.m.
New Global Shutter CMOS Imager with 2 Transistors per Pixel, M. Funaki, T. Shimizu, S. Orihara, H. Kawanaka, M. Kurihara, H. Sato, N. Katsumata, M. Oikawa, J. Higuchi, K. Oe, R. Kuga, K. Maki, T. Nishibata, Victor Company of Japan, Japan

We present a new global shutter CMOS imager with 2 transistors per pixel. The first transistor is a ring gate transistor for accumulating holes that modulate threshold voltage. The second one is a transfer gate transistor that transfers holes from a PD to the ring gate transistor at the same time in all pixels. Simple structure allows us to realize 5.4um pixel pitch, kTC noise free, and global shutter sensor using 0.35um technology.

20.2 - 3:50 p.m.
35-nm Gate-Length and Ultra Low-Voltage (0.45 V) Operation Bulk Thyristor-SRAM/DRAM (BT-RAM) Cell with Triple Selective Epitaxy Layers (TELs), T. Sugizaki, M. Nakamura, M. Yanagita, M. Shinohara, T. Ikuta, T. Ohchi, K. Kugimiya, S. Kanda, K. Yagami, T. Oda, Sony Corporation, Japan

We have successfully developed an alternative SRAM cell using a Bulk Thyristor-RAM (BT-RAM), which has a 35-nm gate-length with Triple selective Epitaxy Layers (TELs) for the anode, the n-base, and the cathode. The TEL BT-RAM reads and writes at an ultra low voltage of 0.45 V at 900 ps and reads and writes at a high speed of 100 ps at 0.9 V. It also has excellent scalability, a high Ion/Ioff ratio, and good thermal stability even at 125 oC. The TEL BT-RAM is therefore a promising alternative SRAM cell for the 35-nm gate length generation and beyond.

20.3 - 4:15 p.m.
Band Offset FinFET-Based URAM (Unified-RAM) Built on SiC for Multi-Functioning NVM and Capacitorless 1T-DRAM, J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, S.-J. Choi, K.J. Choi*, B.J. Cho, J.S. Kim**, K.H. Kim**, G.S. Lee**, J.S. Oh**, M.H. Song**, Y.C. Park**, J.W. Kim**, Y.-K. Choi, KAIST, *Jusung Engineering, **National Nanofab Center, Korea

A FinFET-based unified-RAM (URAM) using the band offset of Si/SiC is demonstrated for the fusion of a non-volatile memory (NVM)and capacitorless 1T-DRAM operation. An oxide/nitride/oxide (O/N/O)gate dielectric and a floating body caused by the band offset are combined in a bulk FinFET to allow two memory operations in a single transistor.