SESSION 21 – HONOLULU SUITE
High Mobility Devices

Thursday, June 19, 3:25 p.m.
Chairpersons: A. Lacaita, Politecnico di Milano
C. Wann, TSMC

21.1 - 3:25 p.m.

PAPER WITHDRAWN BY AUTHOR REQUEST

21.2 - 3:50 p.m.
Integrated Wafer-Scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned-Carbon-Nanotube-Immune Logic Structures, N. Patil, A. Lin, E. Myers, H.-S.P. Wong, S. Mitra, Stanford University, USA

We successfully demonstrate essential components and their integration for large-scale Carbon Nanotube Field Effect Transistor (CNFET) technology: 1. First demonstration of full-wafer-scale growth of directional carbon nanotubes (CNTs) on 4" single-crystal quartz wafers. 2. First demonstration of full-wafer-scale CNT transfer from 4" quartz wafers to 4" silicon wafers for integration on silicon. 3. Integration of full-wafer-scale growth and transfer, together with metallic-CNT removal, for the first demonstration of misaligned-CNT-immune digital logic structures on a full-wafer-scale. Such logic structures guarantee correct logic functionality in the presence of a large number of misaligned and mis-positioned CNTs.

21.3 - 4:15 p.m.
Performance Enhancement Schemes Featuring Lattice Mismatched S/D Stressors Concurrently Realized On CMOS Platform: *e*-SiGeSn S/D For pFETS By Sn^+ Implant And Sic S/D For nFETS By C^+ Implant, G.H. Wang, E.-H. Toh, X. Wang*, D.H.L. Seng**, S. Tripathy**, T. Osipowicz, T.K. Chan, G. Samudra, Y.-C. Yeo, National University of Singapore, *Singapore Institute of Manufacturing Technology, **Institute of Materials Research and Engineering, Singapore

We report, for the first time, a simple and cost effective co-integration of strained p and n-FETs using Tin (Sn) and mono-carbon (C) implant in Source/Drain (S/D) of p- and n-FETs, respectively, to induce beneficial strain. For the first time, a single laser anneal step was employed to substitutionally incorporate the Sn and C atoms simultaneously into lattice sites. 7 at.% substitutional Sn concentration (the equivalent of adding 35% Ge to SiGe S/D stressors) was achieved in the Si0.7Ge0.3S/D of Si channel p-FET. A significant enhancement of up to 150% in hole mobility and 71% in drive current for a 50nm gate length device was observed.