2008 VLSI Technology Short Course
TAPA I/II

CMOS Logic – Technology Challenges for the Transition from 32nm to 22nm

Monday, June 16, 8:10 a.m.

Organizers: Klaus Schruefer, Infineon Technologies
Satoshi Inaba, Toshiba Corporation
Digh Hisamoto, Hitachi Ltd.

8:10 a.m.	**Introduction** K. Schruefer, Infineon Technologies
8:15 a.m.	**Lithography Solutions** M. Colburn, IBM Corporation
9:25 a.m.	**FEOL Scaling, New Device Architectures and Materials** J. Kavalieros, Intel Corporation
10:35 a.m.	**Break**
10:50	**Interconnect Scaling, Processes and Integration** H.-J. Barth, Infineon Technologies
12:00 p.m.	**Lunch**
1:30 p.m.	**System on Chip – Key Aspects for MS/RF Integration** M. Huang, Freescale
2:40 p.m.	**Break**
2:55 p.m.	**Embedded Memory: SRAM** Y. Kim, Samsung Electronics
4:05 p.m.	**Variability and DFM** H. Yoshimura, Toshiba Corporation
5:15 p.m.	**Conclusion**