

Analog/Mixed Signal Design in digital CMOS

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Mixed-signal design in scaled CMOS technologies is increasingly difficult using long-established practices. Lower power supply voltages and larger device mismatch reduce circuit options and degrade performance. Lithography concerns limit the sizes of available devices and their placement. Transistor effects such as xBTI and gate leakage become prominent concerns. Narrow, closely-spaced wires result in larger RC delays, dangerous coupling, and exponentially increasing EM failures. Fortunately, scaled CMOS technologies offer one great benefit to the mixed-signal designer: nearly unlimited digital transistors. These transistors may be used to build all-digital PLLs and DLLs. They allow us to replace large analog filters with compact, digital ones. Most important, these "free" transistors allow us to detect and digitally correct non-idealities in our analog circuits, gaining back lost performance and offering new possibilities for real-time calibration and programmability. These new challenges and opportunities will be explored with real-world examples from 32nm and 45nm mixed-signal designs.