

## **Architecture Trends and Requirements for Wireless RF PLLs, by Chih-Ming Hung, TI Dallas**

RF frequency synthesizers are one of the most critical parts of system-on-chip (SoC) solutions in wireless applications. As CMOS processes scale down, size, raw transistor speed and power consumption dramatically improve on one hand, but difficulties arise in implementing traditional phase-locked loop architectures on the other hand. The challenges include low voltage headroom, high flicker noise, inferior transistor characteristics, highly nonlinear device properties, poor device mismatch, and limited isolation from digital logic. This presentation will first review the new architectural opportunities and challenges in light of the current and emerging wireless standards. It will then focus on recently developed all digital and digitally intensive architectures that are amenable to nanometer-scale process technologies. The remaining 'analog' content, whether understood as continuous-amplitude or continuous-time circuits, is assisted by ultra-fast yet inexpensive digital logic, which runs mostly automatically in the background. Examples of these services will be illustrated, which include calibration for process spread as well as real-time compensation for environmental changes, performance tuning, automatic reconfigurability, and built-in self-test.