

3D/Chip-Package-Co-design

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The presentation reviews the fundamentals in Chip-Package Co-design with emphasis on the optimization of package conductors to minimize the inductances of supply lines and the optimization of their impedance profile to avoid chip-package anti-resonance in modern low-voltage VLSI chips. Due to reduced on-die resistances for lower voltage operation, antiresonance potential is becoming higher and higher. By illustrating multiple current loops in power delivery circuits including board and decoupling capacitors, the mechanism producing antiresonance and preferred countermeasures are presented. Learn inductance dominant power delivery environment just outside of pads on die to avoid catastrophic antiresonance due to capacitance of your chip and external inductances. Other techniques and methodologies for chip-package-board co-design are also described. Pin assignment for DDR2/3 interfaces are presented as typical examples for board first design flow to develop cost effective packages for competitive SoCs. Electro magnetic interference reduction is also discussed in this perspective.