SESSION 15 – HONOLULU SUITE
High-Resolution and High Speed Data Converters

Thursday, June 17, 3:25 p.m.
Chairperson: J. Gealow, MediaTek Wireless, Inc.
S. Dosho, Panasonic Corporation

15.1 - 3:25 p.m.
A 14b 200MS/s DAC with SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist Band enabled by Dynamic-Mismatch Mapping, Y. Tang, J. Briaire*, K. Doris*, R. van Veldhoven*, P. van Beek, H. Hegt, A. van Roermund, Eindhoven University of Technology, The Netherlands, *NXP, The Netherlands

A 14-bit 200MS/s current-steering DAC with a novel digital calibration technique called dynamic-mismatch mapping (DMM) is presented. Compared to traditional static-mismatch mapping and dynamic element matching, DMM reduces the nonlinearities caused by both amplitude and timing errors, without noise penalty. This 0.14µm CMOS DAC achieves a state-of-the-art performance of SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist band.

15.2 - 3:50 p.m.
A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS, Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium

A 0.4mm^2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 0.68/0.5/0.28/0.27/0.41pJ/conv.

15.3 - 4:15 p.m.
A 0.02mm² 65nm CMOS 30MHz BW All-Digital Differential VCO-Based ADC with 64dB SNDR, J. Daniels, W. Dehaene, M. Steyaert, Andreas Wiesbauer*, K.U. Leuven, Belgium, *Infineon Technologies, Austria

A 300MHz all-digital differential VCO-based ADC occupies 0.02mm² in 65nm CMOS, achieving a peak SFDR of 79dB and an SNDR of 64dB over a 30MHz BW. This high linearity is obtained using two VCOs in differential configuration in combination with an 11-points digital calibration. The power consumption is 11.4mW and the FOM is 150fJ/conv. step.

15.4 - 4:40 p.m.
A 12-GS/s 81-mW 5-Bit Time-Interleaved Flash ADC with Background Timing Skew Calibration, M. El-Chammas, B. Murmann, Stanford University, USA

A 12-GS/s 5-bit time-interleaved flash ADC is realized in 65-nm CMOS. The design utilizes a background timing skew calibration technique to improve dynamic performance, and comparator offset calibration to reduce power dissipation. The experimental prototype achieves an SNDR of 25.1 dB at Nyquist and 27.5 dB for low frequency inputs. The circuit occupies an active area of 0.44 mm^2 and consumes 81 mW from a 1.1-V supply.

15.5 - 5:05 p.m.
A CMOS 6-Bit 16-GS/s Time-Interleaved ADC with Digital Background Calibration, C.-C. Huang, C.-Y. Wang, J.-T. Wu, National Chiao Tung University, Taiwan

An 8-channel 6-bit 16-GS/s time-interleaved ADC was fabricated using a 65nm CMOS technology. Each A/D channel is a flash ADC using latch-type comparator with background offset calibration. Timing skews among the channels are also continuously calibrated in the background. The chip achieves 42.3dB SFDR and 30.8dB SNDR at 16 GS/s sampling rate.