SESSION 16 – TAPA I
**Digital Processors**

Friday, June 18, 8:30 a.m.
Chairperson: J. Farrell, Advanced Micro Devices
H. Kabuo, Panasonic Corporation

**16.1 - 8:30 a.m.**
**Fine Grained Power Analysis and Low-Power Techniques of a 128GFLOPS/58W SPARC64™ VIIIfx Processor for Peta-scale Computing,** H. Okano, Y. Kawabe*, R. Kan, T. Yoshida, I. Yamazaki, H. Sakurai, M. Hondou, N. Matsui, H. Yamashita, T. Nakada, T. Maruyama, T. Asakawa, Fujitsu Limited, *Fujitsu Laboratories Limited, Japan

An 8-core SPARC64™ VIIIfx processor is fabricated in a 45nm CMOS process and achieves a peak performance of 128GFLOPS. Measured results show that the processor consumes only 58W of power when executing a maximum power program. Fine-grained power analysis was used to tune the micro-architecture for low power consumption, and circuit-level low-power techniques were developed. Water cooling and supply voltage adjustment contribute to power reduction at the system level.

**16.2 - 8:55 a.m.**
**53Gbps Native GF$(2^4)^2$ Composite-Field AES-Encrypt/Decrypt Accelerator for Content-Protection in 45nm High-Performance Microprocessors,** S. Mathew, F. Sheikh, A. Agarwal, M. Kounavis, S. Hsu, H. Kaul, M. Anders, R. Krishnamurthy, Intel Corporation, USA

An on-die, reconfigurable AES encrypt/decrypt hardware accelerator is fabricated in 45nm CMOS, targeted for content-protection in high-performance microprocessors. Compared to conventional AES implementations, this design computes the entire AES round in native GF$(2^4)^2$ composite-field with one-time GF$(2^8)$-to-GF$(2^4)^2$ mapping cost amortized over multiple AES iterations. This approach along with a fused Mix/InvMixColumns circuit and folded ShiftRow datapath results in 20% area savings and 67% reduction in worst-case interconnect length, enabling AES-128/192/256 ECB block throughput of 53/44/38Gbps, 125mW power measured at 1.1V, 50°C.

**16.3 - 9:20 a.m.**
**A 530Mpixels/s 4096x2160@60fps H.264/AVC High Profile Video Decoder Chip,** D. Zhou, J. Zhou, X. He, J. Kong*, J. Zhu*, P. Liu*, S. Goto, Waseda University, Japan, *Shanghai Jiao Tong University, Japan

An H.264/AVC HP video decoder is implemented in 90nm CMOS. Its maximum throughput reaches 4096x2160@60fps, which is at least 4.3x higher than the state-of-the-art. By using partial MB reordering and lossless frame recompression, 51% of DRAM bandwidth is reduced which results in 58% DRAM power saving. Meanwhile, various efficient parallelization techniques contribute to a core energy saving of 54%.

**16.4 - 9:45 a.m.**
**Power Reduction Schemes in Next Generation Intel® ATOM™ Processor Based SoC for Handheld Applications.,** R. Islam, A. Sabbavarapu, R. Patel, Intel Corporation, USA

Lincroft, the next generation Intel® ATOM™ processor based SoC specifically designed for smartphones, is fabricated in 45nm Hi-K metal gate CMOS. As part of the extensive low power methodology, the chip is divided into numerous power domains with on die distributed powergates to reduce both active and standby power. Measured data shows upto 50X reduction in standby power. Silicon data shows DRAMatically low power in sleep and deeper sleep standby power states.