SESSION 19 – TAPA II
Digital Chip-to-Chip and On-Die Interfaces

Friday, Juen 18, 10:25 a.m.
Chairperson: A. Bhavnagarwala, IBM TJ Watson Research Center
R. Woo, MPA Group LG Electronics

19.1 - 10:25 a.m.
A 2.5kV Isolation 35kV/us CMR 250Mbps 0.13mA/Mbps Digital Isolator in Standard CMOS with an On-Chip Small Transformer, S. Kaeriyama, S. Uchida*, M. Furumiya*, M. Okada*, M. Mizuno, NEC Corporation, Japan, *NEC Electronics Corp., Japan

An on-chip transformer-based digital isolator for intelligent power management (IPM) systems is proposed. It greatly reduces the number of chips in IPM systems by allowing integration of isolators in a CMOS chip together with MPUs or gate drivers. With a proposed pulse generation / detection scheme that enables a 5V standard CMOS transistor to utilize GHz-band signals, transformer area is reduced to 1/4~1/8 that of conventional transformers.

19.2 - 10:50 a.m.
Simultaneous 6Gb/s Data and 10mW Power Transmission using Nested Clover Coils for Non-Contact Memory Card, Y. Yuan, A. Radecki, N. Miura, L.I. Aikawa, Y. Take, H. Ishikuro, T. Kuroda, Keio University, Japan

This paper presents a non-contact memory card and a host employing simultaneous data and power transmission through inductive coupling. Nested clover-shaped data coils are proposed for reducing interference from a power link. The host wirelessly tracks current consumption of the card and adjusts transmit power to improve power transfer efficiency. The prototype is implemented in 65nm CMOS. It achieves 6Gb/s data rate and almost 10% power transfer efficiency over a 100-2k ohm range of the load.

19.3 - 11:15 a.m.
A 0.7V 20fJ/bit Inductive-Coupling Data Link with Dual-Coil Transmission Scheme, N. Miura, T. Shidei, Y. Yuxiang, S. Kawai, K. Takatsu, Y. Kiyota, Y. Asano, T. Kuroda, Keio University, Japan

This paper presents a 20fJ/bit inductive-coupling data link and a 135fJ/cycle clock link operating at 0.7V supply voltage. A dual-coil transmission scheme reduces a number of stacked transistors in a transmitter, enabling low-voltage and hence low-power operation. A test chip is fabricated in 65nm CMOS whose nominal supply voltage is 1.2V. A data rate of 1.1Gb/s and a clock rate of 3.3GHz, both with an error rate <10-12, are achieved at the 0.7V supply voltage.

19.4 - 11:40 a.m.
2.4GHz 7mW All-Digital PVT-Variation Tolerant True Random Number Generator in 45nm CMOS, S. Srinivasan, S. Mathew, R. Ramanarayanan, F. Sheikh, M. Anders, H. Kaul, V. Erraguntla, R. Krishnamurthy, G. Taylor, Intel Corporation, USA

An all-digital True Random Number Generator is fabricated in 45nm CMOS with 2.4Gbps random bit throughput and total power consumption of 7mW. Two-step coarse/fine-grained tuning with a self-calibrating feedback loop enables robust operation in the presence of 20% process variation while providing immunity to run-time voltage and temperature fluctuations. The 100% digital design enables a compact layout occupying 4004µm2 with measured entropy of 0.999965, and scalable operation down to 280mV, while passing all NIST RNG tests.