SESSION 23 – TAPA II
Low-Power Nyquist ADCs

Friday, June 18, 3:40 p.m.
Chairperson: U. Moon, Oregon State University
M. Yoshioka, Fujitsu Laboratories Ltd.

23.1 - 3:40 p.m.
A Zero-Crossing Based 12b 100MS/s Pipelined ADC with Decision Boundary Gap Estimation Calibration, J. Chu, L. Brooks*, H.-S. Lee, Massachusetts Institute of Technology, *Ubixum, Inc., USA

This paper describes a 12-bit zero-crossing based pipeline 100-MS/s ADC. The prototype ADC, fabricated in a 90-nm CMOS process, occupies 0.32 mm2. The capacitor mismatch is calibrated by decision boundary gap estimate algorithm that runs in the background. It achieves an ENOB of 10.2 bits for a 49 MHz input signal and dissipates 6.2 mW from a 1.2V supply for a FOM of 53fJ/step.

23.2 - 4:05 p.m.
A 12b 50MS/s 3.5mW SAR Assisted 2-Stage Pipeline ADC, C. Lee, M. Flynn, University of Michigan, USA

A 12b 50MS/s ADC is presented that pipelines a first stage 6b MDAC with a second stage 7b SAR ADC. The first stage uses a low-power SAR architecture for the sub-ADC, to achieve the large 6b stage resolution. A “half-gain” MDAC reduces the output swing and increases the closed-loop bandwidth of the op-amp in the first stage. This ADC consumes 3.5mW power, achieves an ENOB of 10.4b at Nyquist, and an FOM of 52fJ/conversion-step.

23.3 - 4:30 p.m.
A 1V 11fJ/Conversion-Step 10bit 10MS/s Asynchronous SAR ADC in 0.18µm CMOS, C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang*, National Cheng Kung University, Taiwan, *Himax Technologies, Inc., Taiwan

This paper presents a 10-bit SAR ADC using a variable window function to reduce the unnecessary switching in DAC network. At 10-MS/s and 1-V supply, the ADC consumes only 98µW and achieves an SNDR of 60.97 dB, resulting in an FOM of 11 fJ/Conversion-step. The prototype is fabricated in a 0.18µm CMOS technology.

23.4 - 4:55 p.m.
A 9-bit 150-MS/s 1.53-mW Subranged SAR ADC in 90-nm CMOS, Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, Y.-T. Shyu, S.-J. Chang, National Cheng Kung University, Taiwan

This paper reports a subranged SAR ADC consisting of a 3.5-bit flash coarse ADC, a 6-bit SAR fine ADC, and a differential segmented capacitive DAC. The segmented DAC improves DNL during MSB transitions. The merged switching of MSB capacitors enhances operation speed. The 9-bit 150-MS/s ADC consumes 1.53 mW from a 1.2-V supply. The ENOB is 8.69 bit, the ERBW is 100 MHz, and the FOM is 24.7 fJ/conversion-step.