SESSION 3 – HONOLULU SUITE
UWB Circuits

Wednesday, June 16, 10:25 a.m.
Chairperson: A. Cathelin, STMicroelectronics
J. Lee, National Taiwan University

3.1 - 10:25 a.m.
A 112Mb/s Full Duplex Remotely-Powered Impulse-UWB RFID Transceiver for Wireless NV-Memory Applications, M. Pelissier, B. Gomez, G. Masson, S. Dia, M. Gary, J. Jantunen*, J. Arponen*, J. Vartera*, CEA-LETI - Minatec, France, *Nokia, Finland

A dual band symmetrical RFID transceiver for high capacity wireless NV-memory applications is reported. The circuit exhibits a FOM of 58pJ/b and 48pJ/b in Tx and Rx respectively, with a 112Mb/s data rate capability. It operates in the 7.9GHz UWB frequency band for full duplex communication and is remotely powered thru a UHF CW. The circuit is fabricated in a 0.13µm 1.2V CMOS process.

3.2 - 10:50 a.m.
A Charge-Domain Auto- and Cross-Correlation Based IR-UWB Receiver with Power- and Area-Efficient PLL for 62.5ps Step Data Synchronization in 65nm CMOS, L. Liu, T. Sakurai, M. Takamiya, University of Tokyo, Japan

A 100Mb/s, 1.71mW DC-960MHz band impulse radio ultra-wideband (IR-UWB) receiver is developed in 1.2V 65nm CMOS. A novel auto- and cross-correlation based synchronization scheme is proposed to achieve 62.5ps step data synchronization with a 2-GHz 8-phase PLL clock generator. The developed UWB receiver with the proposed power- and area-efficient PLL achieves the low energy consumption of 17.1pJ/bit.

3.3 - 11:15 a.m.
A 2.4GHz Wireless Transceiver with 0.95nJ/b Link Energy for Multi-Hop Battery-Free Wireless Sensor Networks, J. Ayers, N. Panitantum, K. Mayaram, T. Fiez, Oregon State University, USA

An ultra-low power transceiver for battery-free wireless sensor networks is presented. The receiver uses a modified super-regenerative architecture with BFSK modulation to improve speed and sensitivity. Transmitter efficiency is improved by using a power oscillator to directly drive the antenna. The entire transceiver achieves a total link energy less than 1nJ/b and can communicate over distances as large as 20m, making it the lowest power integrated transceiver to date.

3.4 - 11:40 a.m.
A Fully Integrated, 300pJ/b, Dual Mode 65nm CMOS Transceiver for cm-Range Wireless Links, S. Gambini, J. Crossely, E. Alon, J. Rabaey, University of California, Berkeley, USA

A transceiver for ultra-short range wireless links uses a dual-mode RX architecture to achieve interference robustness at ultra-low power. A direct-AM detection architecture with high-pass baseband filter suppresses out-of-band interferers, and is reconfigured to a mixer-high-pass filter cascade to reject in-band blockers based on real-time BER estimates. At 1Mbps the receiver consumes 300µW and operates with an SIR of 13dB (referred to peak power).