2010 VLSI Circuits Short Course Program
Honolulu II

Frequency Synthesis and Clock Generation

Tuesday, June 15, 8:30 a.m.

Organizers/Chairs: Andreia Cathelin, STMicroelectronics
Shin'ichiro Mutoh, NTT

8:30 a.m.	**Introduction** Andreia Cathelin, STMicroelectronics
8:45 a.m.	**Basics of Jitter and Phase Noise** Asad Abidi, UCLA
9:45 a.m.	**Modeling/Simulation of Large Signal Phenomena in PLL** Rick Poore, Agilent EEs of EDA
10:45 a.m.	**Break**
11:00 a.m.	**Architecture Trends and Requirements for Wireless RF PLLs** Chih-Ming Hung, Texas Instruments
12:00 p.m.	**Lunch**
1:00 p.m.	**Low Power Frequency Synthesis Using BAW/IC Integration** Brian Otis, University of Washington
2:00 p.m.	**Clocking Techniques for High-speed Wireline** Jae-Yoon Sim, POSTECH
3:00 p.m.	**Break**
3:15 p.m.	**Mm-wave PLL Design** Toshiya Mitomo, Toshiba Corp.
4:15 p.m.	**Round Table (all the speakers)** Shin'ichiro Mutoh, NTT
5:00 p.m.	**Conclusion**