CMOS Logic and Embedded Memory Design (NAE)

Kevin Zhang, Intel Corp

The presentation will focus on the state-of-the-art circuit techniques in overcoming these challenges while continuing to achieve the scaling benefits based on Moore's law. For digital circuit design, the presentation will cover several key design techniques in great details, including power-gating, thermal management, and adaptive on-die voltage-frequency scaling to achieve optimal power-performance results. Design examples from most recent high-performance microprocessors will be used to illustrate these design techniques and benefits. As embedded memory design has become increasingly important to today's VLSI applications, this presentation will discuss the latest advancement in combating variation and leakage power for both large on-die SRAM/cache memory and high-performance and low-power embedded multiport arrays. Many latest circuit techniques, including multi-VCC, power management, peripheral circuit design for improving Read/Write margins, will be thoroughly presented along with real design examples.