2010 VLSI TECHNOLOGY SYMPOSIUM HONOLULU

ANNOUNCEMENT AND CALL FOR PAPERS

Sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics
In Cooperation with the IEEE Solid State Circuits Society

2010 SYMPOSIUM ON VLSI TECHNOLOGY

Hilton Hawaiian Village, Honolulu, Hawaii
June 15 - 17, 2010

The 2010 Symposium on VLSI Technology welcomes the submission of papers on all aspects of VLSI technology. In addition, two new topics are added to the scope of the symposium – "Design Enablement" to encourage submissions from Fabless/Fablite and Foundry companies, and "Heterogeneous Integration" of non-Si substrate/materials on large Si wafers for both Moore's Law extension and opportunities orthogonal to conventional scaling (More-Than-Moore). These topics will also be addressed in the Focus Sessions.

FOCUS SESSIONS

Two Focus sessions of exclusively invited papers will cover a selection of key developments in the aforementioned two topics. Design Enablement will focus on how new or disruptive device, process and materials technologies will impact circuit design (including design rule restrictions, device models, OPC, DFM...etc), product performance, and product migratability. Heterogeneous Integration will focus on integrating non-Si substrates/materials on large Si wafers (CNT, graphene, Ge, SiGe, III-V...etc), including their process integration, device architectures, performance and impact on CMOS roadmaps.

The scope of the symposium is being expanded to cover the following topics:

- New concepts and breakthroughs in VLSI devices and processes including Memory, Logic, I/O, and I/F (RF/Analog/Mixed-Signal/High-Voltage, Imager, MEMS, etc.)
- Advanced gate stacks and interconnects in VLSI processes and devices
- Advanced lithography and fine-patterning technologies for high-density VLSI
- New functional devices beyond CMOS with a path for VLSI implementation
- Packing of VLSI devices including 3D-system integration
- Advanced device analysis, materials and modeling for VLSIs
- Reliability related to the above devices
- Theories and fundamentals related to the above devices
- New concepts and technologies for VLSI manufacturing
- Design enablement (including technology impacts on circuit design in advanced CMOS nodes)
- Heterogeneous integration of non-Si substrates/materials on Si substrate

SUBMISSION OF PAPERS

Prospective authors must submit papers in the format of two pages of camera-ready copy to the web page:

http://www.vlsisymposium.org

Please note that hard copy submission will NOT be accepted

Those interested in submitting papers should access the above web site.
The papers are to be submitted in final form and, if accepted, will be published as submitted.

To improve the probability for acceptance of a submitted paper, the paper should describe original work with specific results from experiments or simulations. **The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium.**

Submissions from universities are encouraged. Partial travel expense support for students who are presenting papers is available upon request.

BEST STUDENT PAPER AWARD

The selection will be based upon the quality of the written paper and the presentation. The student who receives the Best Student Paper Award will be presented a monetary award and a certificate at the opening session of the 2011 Symposium. The student must be the leading author and the presenter of the paper, and must indicate in the web submission form that this is a student paper in order to be considered for this award.

Paper Submission Deadline is January 25, 2010, 5:00 P.M. PST

INFORMATION AND REGISTRATION

Prospective attendees can obtain further information and forms for registration and hotel reservations from the Symposium website by visiting www.vlsisymposium.org or from the closest secretariat.

VLSI TECHNOLOGY SHORT COURSE

A one-day short course will be held on June 14, 2010. Details will be given in the VLSI Technology Symposium Advance Program, which will be posted on the web by the middle of April, 2010.

SATELLITE WORKSHOP

2010 Silicon Nanoelectronics Workshop will be held on June 13-14, 2010 at the same location.

Following the first day of this Symposium, the 2010 Symposium on VLSI Circuits will be held at the same location with two days of overlap between the two symposia. See the reverse side.

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