Advance Program

as of May 18, 2011

SYMPOSIUM ON VLSI CIRCUITS

2011

June 15 - 17, 2011
Rihga Royal Hotel Kyoto
Kyoto, Japan

VLSI CIRCUITS SHORT COURSE / WORKSHOP

June 14, 2011

SPONSORED BY

The Japan Society of Applied Physics

The IEEE Solid-State Circuits Society

IN COOPERATION WITH

The Institute of Electronics, Information and Communication Engineers

The IEEE Electron Devices Society

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Early Registration: May 10, 2011

Late Registration: May 31, 2011

Hotel Reservation: May 13, 2011

Welcome to the 2011 Symposium on VLSI Circuits

You are cordially invited to attend the 2011 Symposium on VLSI Circuits, to be held on June 15-17th, 2011, at the Rihga Royal Hotel Kyoto in Kyoto, Japan. We are repeating last year's successful two days' overlap with the Technology Symposium to foster greater interactions and synergies between these two key conferences. This juxtaposition is a unique feature and value that distinguishes the Symposia from other conferences. The Symposium brings together experts and experienced engineers and scientists from industry and academia around the world to discuss present and future challenges in VLSI Circuits and Technology.

Preceding the Circuits Symposium, a one-day Short Course will be held on June 14th. This short course will focus on "Design Awareness in Circuit Design" where experts will give educational talks on this timely topic of challenges and solutions for VLSI circuit designs in scaled CMOS process technology nodes. On the same day, we also have a Workshop on "Bio Inspired Computation - What Electronics can Learn from Bio." For a single Short Course/Workshop registration fee, attendees have access to either parallel session. On the 2nd day of the conference, a luncheon talk entitled "Recent Studies about Computer-Aided Origami Design" will entertain attendees with creative ideas of paper folding, from viewpoints of traditional folk art in Japan and computational sciences towards modern art.

This year, the technical program committee reviewed 409 papers and selected 115 papers for presentation covering a range of topics from Digital Circuits and Systems, Power Management, Memories, Analog, Data Converters, Wireless and Wireline Communications, Sensors, Bio and Medical Electronics. The traditional emphasis of the Symposium has been on paper quality. This year the committee has selected very high quality papers representing the scope of the Symposium. We have also invited four distinguished speakers to describe recent advances and new challenges in the areas of Space Science and Electronics, Medical and Healthcare Services, Computing, and Wireless Communication. To complement the plenary talks and papers, we have arranged two evening sessions on interesting and provocative topics to give you an opportunity to participate in the discussions and mix with the conference attendees. The evening sessions explore: "Non-Volatile Memory (NVM) Technology and New Application Opportunities" and "Will Circuit Design be a Key Issue in Biomedical Applications? (or Boring Circuits?)". The rich technical content of the program will undoubtedly interest you, and we certainly hope that the Symposium will be a fruitful and enjoyable experience. This booklet contains the advance program together with forms for Symposium registration and hotel reservations. Please complete and return these forms or visit our website for online registration at http://www.vlsisymposium.org . Although on-site registration will be available at the conference, pre-registration will facilitate Symposium planning.

We look forward to meeting with you at the Symposium in Kyoto.

Makoto Nagata	Vivek De
Program Chair	Program Co-Chair

CONFERENCE SCHEDULE

Tuesday, June 14	20:00-22:00	Joint Rump Session [Suzaku I, II]	
Wednesday, June 15			
	8:30-10:05	Session 1	**Plenary Session I [Suzaku I, II]**
	10:30-12:35	Session 2	**Switching DC-DC Converters [Suzaku I]**
		Session 3	**Advanced Wireless Transceivers [Suzaku II]**
		Session 4	**Oversampling Converters [Suzaku III]**
	12:35-13:55	Lunch	
	13:55-16:00	Session 5	**Circuit and System Integration [Suzaku I]**
		Session 6	**High Performance DACs and Amplifiers [Suzaku III]**
	13:55-16:00	Highlights (Technology) [Shunju]	
	16:10-17:50	Session 7	**Embedded SRAM and Applications [Suzaku I]**
		Session 8	**Multi Gigabit Wireline Communication [Suzaku II]**
		Session 9	**Image Sensors [Suzaku III]**
	19:00-21:00	Joint Cocktail/Dinner Party	
Thursday, June 16			
	8:45-10:05	Session 10	**Plenary Session II [Suzaku I, II]**
	10:30-12:35	Session 11	**Fractional-N PLLs [Suzaku I]** (10:30-12:10)
		Session 12	**Pipelined ADCs [Suzaku III]**
	12:35-14:20	Lunch	Luncheon Talk [Suzaku II] (12:45-14:05)
	14:20-16:00	Session 13	**High Speed Digital for Interconnects [Suzaku I]**
		Session 14	**Bio Interfaces [Suzaku III]**
	16:15-17:55	Session 15	**Clocking Building Blocks [Suzaku I]**
		Session 16	**Ultra Low Power Transceivers [Suzaku II]**
		Session 17	**Bio Sensors and Applications [Suzaku III]**
	20:00-22:00	Rump Sessions [Suzaku I, II, III]	
Friday, June 17			
	8:30-10:10	Session 18	**High Performance Circuit Techniques [Suzaku I]**
		Session 19	**Nonvolatile Memories [Suzaku II]**
		Session 20	**High Speed and Low Power Receiver Techniques [Suzaku III]**
	10:30-12:35	Session 21	**Device-Based Circuit Techniques [Suzaku I]**
		Session 22	**DRAM and Memory Interfaces [Suzaku II]** (10:30-12:10)
		Session 23	**Power Management for Energy Harvesting [Suzaku III]**
	12:35-13:55	Lunch	
	13:55-16:00	Session 24	**Digital Processors [Suzaku I]**
		Session 25	**Emerging ADCs [Suzaku II]**
		Session 26	**Power Management Technique [Suzaku III]**
	16:15-17:55	Session 27	**Signal Processing for Wireline [Suzaku I]**
		Session 28	**Nonvolatile Memory Applications [Suzaku II]**

PROGRAM

Wednesday, June 15

Session 1		**Welcome and Plenary Session I [Suzaku I, II]**
Chairpersons		M. Nagata, *Kobe Univ.* V. De, *Intel Corp.*
8:30	1-1	**Welcome and Opening Remarks**
Invited		M. Mizuno, *Renesas Electronics Corp.* A. Amerasekera, *Texas Instruments, Inc.*
8:45	1-2	**The Hayabusa Mission - Its Seven Years Flight**
Invited		J. Kawaguchi, *Japan Aerospace Exploration Agency (JAXA), Japan*
9:25	1-3	**The Swarm at the Edge of the Cloud -A New Perspective on Wireless**
Invited		J.M. Rabaey, *University of California at Berkeley, USA*

(Break 10:05-10:30)

Session 2		**Switching DC-DC Converters [Suzaku I]**
Chairpersons		C. Yoo, *Hanyang Univ.* U.-K. Moon, *Oregon State Univ.*
10:30	2-1	**A 50.3ns Transient-Response CR-Free SIMO Power Converter with Adaptive Current Compensation**
		Y. Zhang and D. Ma
		The University of Texas at Dallas, USA
10:55	2-2	**A 98% Cross-Talk Self-Cancellation Single-Inductor Dual-Output DC-DC Converter Using Bidirectional Power Prediction (BPP) Control in 65nm CMOS**
		Y.-H. Lee*, Y.-Y. Yang*, T.-C. Huang*, C.-Y. Hsieh*, K.-H. Chen*, Y.-K. Chen**, C.-C. Huang** and Y.-H. Lin**
		**National Chiao Tung University and **Realtek Semiconductor Corp., Taiwan*
11:20	2-3	**A Single-Inductor 8-Channel Output DC-DC Boost Converter with Time-Limited One-Shot Current Control and Single Shared Hysteresis Comparator**
		J. Kim, D. S. Kim and C. Kim
		Korea University, Korea
11:45	2-4	**Fixed-Frequency Adaptive-On-Time Boost Converter with Fast Transient Response and Light Load Efficiency Enhancement by Auto-Frequency-Hopping**
		X. Jing and P.K.T. Mok
		The Hong Kong University of Science and Technology, China
12:10	2-5	**A Spurious-Free Switching Buck Converter Using a Delta-Sigma Modulation Controller with a Scalable Sampling Frequency**
		M.K. Alghamdi and A.A. Hamoui
		McGill University, Canada

(Lunch 12:35-13:55)

Session 3		Advanced Wireless Transceivers [Suzaku II]
Chairpersons		H. Ishikuro, *Keio Univ.* A. Cathelin, *STMicroelectronics*
10:30	3-1	**A 0.38THz Fully Integrated Transceiver Utilizing Quadrature Push-Push Circuitry**
		J.-D. Park, S. Kang and A.M. Niknejad
		University of California, Berkeley, USA
10:55	3-2	**A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS**
		C. Thakkar*, L. Kong*, K. Jung*, A. Frappé** and E. Alon*
		**University of California, Berkeley, USA and **Institut Supérieur de l'Electronique et du Numérique, France*
11:20	3-3	**A 2.5GHz Delay-Based Wideband OFDM Outphasing Modulator in 45nm-LP CMOS**
		A. Ravi, P. Madoglio, M. Verhelst, M. Sajadieh, M. Aguirre, H. Xu, S. Pellerano, I. Lomeli, J. Zarate, L. Cuellar, O. Degani, H. Lakdawala, K. Soumyanath and Y. Palaskas
		Intel Corporation, USA
11:45	3-4	**A Configurable Multi-Band Multi-Mode Transmitter with Spur Cancellation Through Digital Baseband**
		Y. Tang, M. Chen, W. Leung, C. Narathong, M. Ranjan, K. Godbole, G. Zhang, O. Choksi, V. Panikkath, C. Holenstein, A. Hadjichristos and K. Sahota
		Qualcomm, USA
12:10	3-5	**A 3.5mm^2, Inductor-Less Digital-Intensive Radio SoC for 300-to-950MHz ISM-Band Applications Supporting 1.0-to-240kbps Multi-Data-Rates**
		T. Tokairin*, H. Saito**, H. Ishizaki*, Y. Oka*, T. Maeda*, S. Oshima**, M. Soda*, M. Okada*, S. Hori***, M. Kitsunezuka*** and M. Mizuno*
		**Renesas Electronics Corporation, **Renesas Micro Systems Co., Ltd. and ***NEC Corporation, Japan*

(Lunch 12:35-13:55)

Session 4		Oversampling Converters [Suzaku III]
Chairpersons		M. Ito, *Renesas Electronics Corp.* J. Lloyd, *Analog Devices, Inc.*
10:30	4-1	**A 12-ENOB 6X-OSR Noise-Shaped Pipelined ADC Utilizing a 9-bit Linear Front-End**
		O. Rajaee** and U. Moon*
		**Oregon State University and **Qualcomm, USA*
10:55	4-2	**A 32nm, 1.05V, BIST Enabled, 10-40MHz, 11-9 Bit, 0.13mm^2 Digitized Integrator MASH ΔΣ ADC**
		B. R. Carlton, H. Lakdawala, E. Alpman, J. Rizk, Y.W. Li, B. Perez-Esparza, V. Rivera, C.F. Nieva, E. Gordon, P. Hackney, C.-H. Jan, I.A. Young and K. Soumyanath
		Intel Corporation, USA
11:20	4-3	**A Continuous-Time, Jitter Insensitive ∑Δ Modulator Using a Digitally Linearized G_m-C Integrator with Embedded SC Feedback DAC**
		D. Kim*, T. Matsuura** and B. Murmann*
		**Stanford University, USA and **Renesas Electronics Corp., Japan*

11:45	4-4	**A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass ΔΣ ADC for RF Digitization with Integrated PLL and Polyphase Decimation Filter in 40nm CMOS**
		E. Martens, A. Bourdoux, A. Couvreur, P. Van Wesemael, G. Van der Plas, J. Craninckx and J. Ryckaert
		IMEC, Belgium
12:10	4-5	**A 2.8 mW ΔΣ ADC with 83 dB DR and 1.92 MHz BW Using FIR Outer Feedback and TIA-Based Integrator**
		J. Gealow*, M. Ashburn*, C.-H. Lou*, S. Ho*, P. Riehl*, A. Shabra**, J. Silva* and Q. Yu*
		**MediaTek Wireless, Inc., USA and **Masdar Institute of Science and Technology, UAE*

(Lunch 12:35-13:55)

Session 5		**Circuit and System Integration [Suzaku I]**
Chairpersons		C. Hou, *TSMC* J. Barth, *IBM Microelectronics*
13:55	5-1	**Measurement, Analysis and Improvement of Supply Noise in 3D ICs**
		P. Jain, D. Jiao, X. Wang and C.H. Kim
		University of Minnesota, USA
14:20	5-2	**Isolation Techniques Against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) for RF/Mixed-Signal SoCs**
		S. Uemura, Y. Hiraoka, T. Kai and S. Dosho
		Panasonic Corporation, Japan
14:45	5-3	**A Fully-Integrated Cantilever-Based DNA Detection SoC in a CMOS Bio-MEMS Process**
		Y.-J. Huang*, C.-W. Huang*, T.-H. Lin*, C.-T. Lin*, L.-G. Chen*, P.-Y. Hsiao*, B.-R. Wu*, H.-T. Hsueh*, B.-J. Kuo*, H.-H. Tsai**, H.-H. Liao**, Y.-Z. Juang**, C.-K. Wang* and S.-S. Lu*
		**National Taiwan University and **National Applied Research Laboratories, Taiwan*
15:10	5-4	**A 65nm CMOS Movable Parts Manager for Optical Disc System**
		F. Senoue*, K. Okamoto*, S. Sakiyama*, T. Morie*, S. Dosho*, H. Nishino**, K. Tanimoto**, A. Kawabe** and H. Kobayashi**
		**Panasonic Corporation and **Panasonic Corporation Semiconductor Company Corporate, Japan*
15:35	5-5	**20-μW Operation of an a-IGZO TFT-Based RFID Chip Using Purely NMOS "Active" Load Logic Gates with Ultra-Low-Consumption Power**
		H. Ozaki, T. Kawamura, H. Wakana, T. Yamazoe and H. Uchiyama
		Hitachi, Ltd., Japan

(Break 16:00-16:10)

Session 6		High Performance DACs and Amplifiers [Suzaku III]
Chairpersons		J. Lee, *National Taiwan Univ.* M. Flynn, *Univ. of Michigan*
13:55	6-1	**A 100dB DR Ground-Referenced Single-Ended Class-D Amplifier in 65nm CMOS**
		X. Jiang, J. Song, M. Wang, J. Chen, H. Zheng, S. Galal, K. Abdelfattah and T.L. Brooks
		Broadcom Corporation, USA
14:20	6-2	**A Ping-Pong-Pang Current-Feedback Instrumentation Amplifier with 0.04% Gain Error**
		S. Sakunia*, F. Witte**, M. Pertijs* and K. Makinwa*
		**Delft University of Technology and **National Semiconductor, The Netherlands*
14:45	6-3	**A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz f_T BiCMOS Process**
		K. Poulton, B. Jewett and J. Liu
		Agilent Technologies, USA
15:10	6-4	**A 3GS/s, 9b, 1.2V Single Supply, Pure Binary DAC with >50dB SFDR up to 1.5GHz in 65nm CMOS**
		S.L. Tual*, P.N. Singh*,***, A. Bal** and C. Garnier*
		**STMicroelectronics Crolles, France, **STMicroelectronics G. Noida, India and ***Wolfson Microelectronics Edinburgh, UK*
15:35	6-5	**A 10b 600MS/s Multi-Mode CMOS DAC for Multiple Nyquist Zone Operation**
		S.Y.-S. Chen, N.-S. Kim and J. Rabaey
		University of California, Berkeley, USA

(Break 16:00-16:10)

Session 7		Embedded SRAM and Applications [Suzaku I]
Chairpersons		M. Yamaoka, *Hitachi America, Ltd.* M. Clinton, *Texas Instruments, Inc.*
16:10	7-1	**A 40nm Fully Functional SRAM with BL Swing and WL Pulse Measurement Scheme for Eliminating a Need for Additional Sensing Tolerance Margins**
		Y.-H. Chen*,**, S.- Y. Chou*, Q. Lee*, W.-M. Chan*, D. Sun*, H.-J. Liao*, P. Wang*, M.-F. Chang** and H. Yamauchi***
		**TSMC, **National Tsing Hua University, Taiwan and ***Fukuoka Institute of Technology, Japan*
16:35	7-2	**A 40-nm 0.5-V 20.1-μW/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme**
		S. Yoshimoto*, M. Terada*, S. Okumura*, T. Suzuki**, S. Miyano**, H. Kawaguchi* and M. Yoshimoto*
		**Kobe University and **Semiconductor Technology Academic Research Center (STARC), Japan*
17:00	7-3	**A Larger Stacked Layer Number Scalable TSV-Based 3D-SRAM for High-Performance Universal-Memory-Capacity 3D-IC Platforms**
		M.-F. Chang*, W.-C. Wu*, C.-S. Lin**, P.-F. Chiu**, M.-B. Chen*,**, Y.-H. Chen*,***, H.-C. Lai**, Z.-H. Lin**, S.-S. Sheu**, T.-K. Ku** and H. Yamauchi****
		**National Tsing Hua University, **ITRI, ***TSMC, Taiwan and ****Fukuoka Institute of Technology, Japan*

17:25	7-4	**A Chip-ID Generating Circuit for Dependable LSI Using Random Address Errors on Embedded SRAM and On-Chip Memory BIST**
		H. Fujiwara, M. Yabuuchi, H. Nakano, H. Kawai, K. Nii and K. Arimoto
		Renesas Electronics Corporation, Japan

(Joint Cocktail/Dinner Party19:00-21:00)

Session 8		**Multi Gigabit Wireline Communication [Suzaku II]**
Chairpersons		K. Sunaga, *NEC Corp.* T. C. Carusone, *Univ. of Toronto*
16:10	8-1	**An 8x10-Gb/s Source-Synchronous I/O System Based on High-Density Silicon Carrier Interconnects**
		T.O. Dickson, Y. Liu, S.V. Rylov, B. Dang, C.K. Tsang, P.S. Andry, J.F. Bulzacchelli, H.A. Ainspan, X. Gu, L. Turlapati, M.P. Beakes, B.D. Parker, J.U. Knickerbocker and D.J. Friedman
		IBM T. J. Watson Research Center, USA
16:35	8-2	**A 5.6Gb/s 2.4mW/Gb/s Bidirectional Link With 8ns Power-On**
		J. Zerbe*, B. Daly*, W. Dettloff*, T. Stone*, W. Stonecypher*, P. Venkatesan*, K. Prabhu*, B. Su*, J. Ren*, B. Tsang*, B. Leibowitz*, D. Dunwell**, A.C. Carusone** and J. Eble*
		**Rambus Inc, USA and **University of Toronto, Canada*
17:00	8-3	**An 8Gb/s Forwarded-Clock I/O Receiver with up to 1GHz Constant Jitter Tracking Bandwidth Using a Weak Injection-Locked Oscillator in 0.13µm CMOS**
		S.-H. Chung*, L.-S. Kim*, S.-J. Bae**, K.-S. Ha**, J.-B. Lee** and J.S. Choi**
		**KAIST and **Samsung Electronics, Korea*
17:25	8-4	**A 0.12mm^2 5Gbps Receiver with a Level Shifting Equalizer and a Cumulative-Histogram-Based Adaptation Engine**
		Y. Tomita*, H. Yamaguchi*, S. Kawahara**, T. Higuchi**, T. Yamamoto*, H. Ishida***, K. Gotoh*** and H. Tamura*
		**Fujitsu Laboratories LTD., **Fujitsu LSI Solutions LTD. and ***Fujitsu Semiconductor LTD., Japan*

(Joint Cocktail/Dinner Party 19:00-21:00)

Session 9		**Image Sensors [Suzaku III]**
Chairpersons		Y. Kato, *Panasonic Corp.* M. Whatley, *Cypress Semiconductor*
16:10	9-1	**A Digital CDS Scheme on Fully Column-Inline TDC Architecture for An APS-C Format CMOS Image Sensor**
		T. Takahashi*, H. Ui*, N. Takatori**, S. Sanada**, T. Hamamoto**, H. Nakayama**, Y. Moriyama*, M. Akahide*, T. Ueno* and N. Fukushima*
		**Sony Corporation and **Sony LSI Design Incorporated, Japan*
16:35	9-2	**A 640×480 Image Sensor with Unified Pixel Architecture for 2D/3D Imaging in 0.11µm CMOS**
		S.-J. Kim, J.D.K. Kim, S.-W. Han, B. Kang, K. Lee and C.-Y. Kim
		Samsung Advanced Institute of Technology, Korea

17:00	9-3	**A Dual In-Pixel Memory CMOS Image Sensor for Computation Photography**
		G. Wan*,**, X. Li*, G. Agranov*, M. Levoy** and M. Horowitz**
		**Aptina, LLC and **Stanford University, USA*
17:25	9-4	**A CMOS ∑-Δ Photodetector Array for Bioluminescence-Based DNA Sequencing**
		R.R. Singh, B. Li, A. Elligton and A. Hassibi
		University of Texas at Austin, USA

(Joint Cocktail/Dinner Party 19:00-21:00)

Thursday, June 16

Session 10		**Plenary Session II [Suzaku I, II]**
Chairpersons		M. Nagata, *Kobe Univ.* V. De, *Intel Corp.*
8:45	10-1	**Circuit Challenges for Future Computing Systems**
Invited		W. J. Dally, *NVIDIA and Stanford Univ., USA*
9:25	10-2	**Smart Devices and Services in Healthcare and Wellness**
Invited		H. Nakajima* and T. Shiga**, **Omron Corporation and **Omron Healthcare Co., Ltd., Japan*

(Break 10:05-10:30)

Session 11		**Fractional-N PLLs [Suzaku I]**
Chairpersons		S.H. Cho, *KAIST* N. Kurd, *Intel Corp.*
10:30	11-1	**A Low Spur Fractional-*N* Digital PLL for 802.11 a/b/g/n/ac with 0.19 ps_{rms} Jitter**
		C.-W. Yao, L. Lin, B. Nissim, H. Arora and T. Cho
		Marvell Semiconductor, Inc. USA
10:55	11-2	**A -104dBc/Hz In-Band Phase Noise 3GHz All Digital PLL with Phase Interpolation Based Hierarchical Time to Digital Convertor**
		D. Miyashita, H. Kobayashi, J. Deguchi, S. Kousai and M. Hamada
		Toshiba Corporation, Japan
11:20	11-3	**A 3.6GHz 1MHz-Bandwidth ΔΣ Fractional-N PLL with a Quantization-Noise Shifting Architecture in 0.18μm CMOS**
		W.-H. Chiu and T.-H. Lin
		National Taiwan University, Taiwan
11:45	11-4	**A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping ΔΣ TDC**
		D.-W. Jee, Y.-H. Seo, H.-J. Park and J.-Y. Sim
		Pohang University of Science and Technology (POSTECH), Korea

(Lunch 12:35-14:20)

Session 12		Pipelined ADCs [Suzaku III]
Chairpersons		S. Dosho, *Panasonic Corp.* C.-M. Hung, *MStar Semiconductor, Inc.*
10:30	12-1	**A 12b 3GS/s Pipeline ADC with 500mW and 0.4 mm^2 in 40nm Digital CMOS**
		C.-Y. Chen and J. Wu
		Broadcom Corporation, USA
10:55	12-2	**An 11b 300MS/s 0.24pJ/Conversion-Step Double-Sampling Pipelined ADC with On-Chip Full Digital Calibration for All Nonidealities Including Memory Effects**
		T. Miki, T. Morie, T. Ozeki and S. Dosho
		Panasonic Corporation, Japan
11:20	12-3	**A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-Bit/Stage Folding Converter Architecture**
		T. Yamase*, H. Uchida** and H. Noguchi*
		**NEC Corporation and **NEC Engineering, Ltd., Japan*
11:45	12-4	**A 10b 320 MS/s 40 mW Open-Loop Interpolated Pipeline ADC**
		M. Miyahara, H. Lee, D. Paik and A. Matsuzawa
		Tokyo Institute of Technology, Japan
12:10	12-5	**A 16-mW 8-Bit 1-GS/s Subranging ADC in 55nm CMOS**
		Y.-H. Chung*,** and J.-T. Wu*
		**National Chiao-Tung University and **MediaTek Inc. Taiwan*

(Lunch 12:35-14:20)

12:45-14:05 (Separate Registration Required)

Luncheon Talk [Suzaku II] Organizer: K. Kobayashi, *Kyoto Institute of Technology*
Recent Studies about Computer Aided Origami Design J. Mitani, *Univ. of Tsukuba* *To register for the Luncheon Talk please refer to the registration form for fee information.

Session 13		High Speed Digital for Interconnects [Suzaku I]
Chairpersons		M. Igarashi, *Sony Corp.* C. Sechen, *Univ. of Texas at Dallas*
14:20	13-1	**The 10G-EPON OLT and ONU LSIs for the Coexistence of 10G-EPON and GE-PON toward the Next FTTH Era**
		M. Urano, T. Kawamura, S. Ohteru, H. Suto, K. Kawai, R. Kusaba, N. Miura, J. Kato, A. Miyazaki, T. Hatano, S. Yasuda, N. Tanaka, S. Shigematsu, M. Nakanishi and T. Shibata
		NTT Microsystem Integration Laboratories, Japan
14:45	13-2	**A 2.37Gb/s 284.8mW Rate-Compatible (491,3,6) LDPC-CC Decoder**
		C.-L. Chen, Y.-H. Lin, H.-C. Chang and C.-Y. Lee
		National Chiao Tung University, Taiwan

15:10	13-3	**A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric**
		C.C. Wang, F.-L. Yuan, H. Chen and D. Marković
		University of California, Los Angeles, USA
15:35	13-4	**SWIFT: A 2.1Tb/s 32×32 Self-Arbitrating Manycore Interconnect Fabric**
		S. Satpathy, R. Dreslinski, T.-C. Ou, D. Sylvester, T. Mudge and D. Blaauw
		University of Michigan, USA

(Break 16:00-16:15)

Session 14		**Bio Interfaces [Suzaku III]**
Chairpersons		C.-Y. Lee, *National Chiao Tung Univ.* K. Chang, *Xilinx*
14:20	14-1	**A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications**
		H. Kim*, R.F. Yazicioglu*, S. Kim*, N. Van Helleputte*, A. Artes**, M. Konijnenburg**, J. Huisken**, J. Penders** and C. Van Hoof*,**,
		**IMEC, Belgium and **IMEC-nl/Holst center, The Netherlands*
14:45	14-2	**A 96-Channel Full Data Rate Direct Neural Interface in 0.13µm CMOS**
		R.M. Walker*, H. Gao*, P. Nuyujukian*, K. Makinwa**, K.V. Shenoy*, T. Meng* and B. Murmann*
		**Stanford University, USA and **Delft University of Technology, The Netherlands*
15:10	14-3	**BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication**
		S.-I. Chang, K. AlAshmouny, M. McCormick, Y.-C. Chen and E. Yoon
		University of Michigan, USA
15:35	14-4	**A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor**
		S. Ayazian*, E. Soenen** and A. Hassibi*
		**University of Texas at Austin and **TSMC, USA*

Session 15		**Clocking Building Blocks [Suzaku I]**
Chairpersons		H.-J. Park, *Pohang Univ. of Science and Technology (POSTECH)* J. Tierno, *IBM TJ Watson Research Center*
16:15	15-1	**A 0.63ps Resolution, 11b Pipeline TDC in 0.13µm CMOS**
		Y.-H. Seo, J.-S. Kim, H.-J. Park and J.-Y. Sim
		Pohang University of Science and Technology (POSTECH), Korea
16:40	15-2	**553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator**
		D. Shim*, D. Koukis*, D.J. Arenas*, D.B. Tanner* and Kenneth K. O.**
		**University of Florida and **University of Texas at Dallas, USA*

17:05	15-3	**High-PSRR All-Digital Delay Locked Loop with Burst Update Mode and Power Noise Damping Scheme**
		Y. Kim, J. Jang, J. Moon, S. Lee, D. Kwon, H. Choi, G. Park and B. Chung
		Hynix Semiconductor, Korea
17:30	15-4	**A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance**
		F.S. Lee*, J. Salvia*, C. Lee**, S. Mukherjee*, R. Melamud*, N. Arumugam*, S. Pamarti***, C. Arft*, P. Gupta*, S. Tabatabaei*, B. Garlepp**, H.-C. Lee*, A. Partridge*, M.H. Perrott**** and F. Assaderaghi*
		**SiTime, **Silicon Laboratories, ***University of California, Los Angeles, USA and ****Masdar Institute, UAE*

Session 16		**Ultra Low Power Transceivers [Suzaku II]**
Chairpersons		K. Agawa, *Toshiba Corp.* J. Savoj, *Xilinx*
16:15	16-1	**A Battery-Less WiFi-BER Modulated Data Transmitter with Ambient Radio-Wave Energy Harvesting**
		H. Ishizaki*, H. Ikeda*, Y. Yoshida**, T. Maeda*, T. Kuroda** and M. Mizuno*
		**Renesas Electronics Corporation and **Keio University, Japan*
16:40	16-2	**315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4µW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS**
		L. Liu, T. Sakurai and M. Takamiya
		The University of Tokyo, Japan
17:05	16-3	**A 550µW Inductorless Bandpass Quantizer in 65nm CMOS for 1.4-to-3GHz Digital RF Receivers**
		D. Lachartre
		CEA, LETI, France
17:30	16-4	**A 1mm^3 2Mbps 330fJ/b Transponder for Implanted Neural Sensors**
		M. Mark, Y. Chen, C. Sutardja, C. Tang, S. Gowda, M. Wagner, D. Werthimer and J. Rabaey
		University of California, Berkeley, USA

Session 17		**Bio Sensors and Applications [Suzaku III]**
Chairpersons		M. Ikeda, *The Univ. of Tokyo* B. Nauta, *Univ. of Twente*
16:15	17-1	**A 0.5-V Sub-mW Wireless Magnetic Tracking Transponder for Radiation Therapy**
		W.-F. Loke*, W.-H. Chen*, T. Maleki*, M.A. Khater*, B. Ziaie*, L. Papiez** and B. Jung*
		**Purdue University and **UT Southwestern Medical School, USA*
16:40	17-2	**A 256 Channel Magnetoresistive Biosensor Microarray for Quantitative Proteomics**
		D.A. Hall*, R.S. Gaster*, S.J. Osterfeld*, K. Makinwa**, S.X. Wang* and B. Murmann*
		**Stanford University, USA and **Delft University of Technology, The Netherlands*

17:05	17-3	**Magnetic Relaxation Detector for Microbead Labels in Biomedical Assays**
		P. Liu, K. Skucha, Y. Duan, M. Megens, J. Kim, I. Izyumin, S. Gambini and B. Boser
		University of California, Berkeley, USA
17:30	17-4	**Low Power Control IC for Efficient High-Voltage Piezoelectric Driving in a Flying Robotic Insect**
		M. Karpelson, R.J. Wood and G.-Y. Wei
		Harvard University, USA

20:00

Rump Sessions	
Organizers	K. Nose, *Renesas Electronics Corp.* K. Chang, *Xilinx*
R-1	**Special Evening Session : NVM Technology and New Application Opportunities [Suzaku I, II]**
Organizers	H. Yamauchi, *Fukuoka Institute of Technology* M. Bauer, *Micron Technology, Inc.*
Moderator	M. Bauer, *Micron Technology, Inc.*
Speakers	**FLASH :** K-T. Park, *Samsung Electronics* **PCM :** E. Doller, *Micron Technology, Inc.* **MRAM :** K. Tsuchida, *Toshiba Corp.* **RRAM :** K. Takeuchi, *The Univ. of Tokyo* **FRAM :** T. Moise, *Texas Instruments*
NAND Flash is the industry incumbent NVM. However new materials either being developed or are in production are frequently being compared to Flash. We need to start considering attributes of all memory types, which applications they are best suited for, and what new applications all NVM types may enable. This session will include five experts representing different NVM technologies: PCM, MRAM, FRAM and RRAM and the incumbent NAND Flash. Each speaker will: 1) describe the memory technology from a cell perspective, then how it works in an array, followed by the resulting characteristics such as latency, power, retention, endurance, and cost. 2) Consider key applications for their technology being explicit about why the technology is the best fit and why a company would be compelled to invest in such a technology. This is not to be a discussion of on which technology is then next NAND replacement. The intent is to answer questions such as: Does the technology a good fit for existing applications? Will it drive new applications? Can one NVM technology complement another for an overall better solution than either one on its own? We consider one technology at a time: Speaker presents his technology for 20 minutes then open the discussion for feedback or opinion from the other four panelists, and finally questions from the audience. Then on to the next topic until all five technologies have been discussed.	
R-2	**Will Circuit Design be a Key Issue in Biomedical Applications? (or Boring Circuits?) [Suzaku III]**
Organizers	A. Cathelin, *STMicroelectronics* M. Takamiya, *The Univ. of Tokyo*
Moderator	A. Cathelin, *STMicroelectronics*
Panelists	J. Ohta, *Nara Institute of Science and Technology* J. Rabaey, *Univ. of California, Berkeley* K. Shepard, *Columbia Univ.* M. Flynn, *Univ. of Michigan* H. Takahashi, *The Univ.of Tokyo* C.-C. Wu, *National Taiwan Univ. Hospital* M. M. Maharbiz, *Univ. of California, Berkeley*

Since one decade now there is growing interest for bio-medical applications among IC designers. Several directions are explored such as:

- improving existing electronics medical aid by miniaturization/ lowering power consumption/ improving reliability
- supporting medical aid in new fields by advanced IC technology
- new exploratory fields that are possible only by advantageous medical and microelectronics joint research

We have assembled a distinguished panel of experts who will discuss and debate on these topics. At the end of the day, the goal of this collaborative panel is to draw answers to the following questions:

- Will circuit design be a key issue in biomedical applications and which IC technology to use?
- Which are the technologies to bring together for succeeding circuits in biomedical field?
- What should circuit designers do in biomedical applications?
- Is consumer product type qualification enough/ sufficient for medical application products?
- Which are the ethic problems to be solved before launching mass production bio-medical products?

20:00-22:00

Joint Rump Session	
Organizers	K. Nose, *Renesas Electronics Corp.* K. Chang, *Xilinx*
Title:	**Low Voltage - How Low can we go with Technology and Design Solutions? [Suzaku I, II]**
Organizers	S. Dosho, *Panasonic Corp.* M. Clinton, *Texas Instruments, Inc.* N. Kasai, *Tohoku Univ.* T. Skotnicki, *STMicroelectronics*
Moderator	K. Ishimaru, *Toshiba Corp.* K. Zhang, *Intel Corp.*
Panelists	F. Boeuf, *STMicroelectronics* B. Calhoun, *Univ. of Virginia* M. Ieong, *TSMC* K. Rim, *IBM Corp.* S. Kosonocky, *AMD* A. Matsuzawa, *Tokyo Institute of Technology* S. Paak, *Samsung* Electronics H. Shinohara, *STARC*

Continually lowering IC voltage levels has been critical to continued device scaling for a long time, but now many circuit designers are finding it increasingly difficult to design robust circuits with the lower voltage levels. Is it possible that Moore's Law will end due to our inability to reduce voltage levels, and not because of our inability to further scale transistors? We have assembled a distinguished panel to debate some of the following questions, and much more:

- What role does technology play in requiring lower operating voltages? What is the role of circuit design?
- Lower operating voltages cause problems (and benefits) for circuit designers, are there technology solutions to some of these problems? Conversely, if voltage levels are not scaled this will cause device problems and is it possible that there are circuit solutions to these technology problems?
- Are voltage levels low enough today, or how much lower can we expect them to go in the future?

***This session will be held at 20:00 - 22:00 on Tuesday, June 14.**

Friday, June 17

Session 18		High Performance Circuit Techniques [Suzaku I]
Chairpersons		H. Kabuo, *Panasonic Corp.* J. Chang, *TSMC*
8:30	18-1	**A 27% Active-Power-Reduced 40-nm CMOS Multimedia SoC with Adaptive Voltage Scaling Using Distributed Universal Delay Lines**
		Y. Ikenaga*, M. Nomura*, S. Suenaga*, H. Sonohara*, Y. Horikoshi*, T. Saito*, Y. Ohdaira**, Y. Nishio***, T. Iwashita**, M. Satou**, K. Nishida*, K. Nose*, K. Noguchi*, Y. Hayashi* and M. Mizuno*
		**Renesas Electronics Corporation, **Renesas Mobile Corporation and ***Renesas Micro Systems Co., Ltd., Japan*
8:55	18-2	**LC^2: Limited Contention Level Converter for Robust Wide-Range Voltage Conversion**
		Y. Kim, D. Sylvester and D. Blaauw
		University of Michigan, USA
9:20	18-3	**Adaptive Robustness Tuning for High Performance Domino Logic**
		B. Giridhar*, D. Fick*, M. Fojtik*, S. Satpathy*, D. Bull**, D. Sylvester* and D. Blaauw*
		**University of Michigan, USA and **ARM, United Kingdom*
9:45	18-4	**A 381 fs/bit, 51.7 nW/bit Nearest Hamming-Distance Search Circuit in 65 nm CMOS**
		H.J. Mattausch, M. Yasuda, A. Kawabata, W. Imafuku and T. Koide
		Hiroshima University, Japan

(Break 10:10-10:30)

Session 19		Nonvolatile Memories [Suzaku II]
Chairpersons		K. Kajigaya, *Elpida Memory, Inc.* M. Bauer, *Micron Technology, Inc.*
8:30	19-1	**A 21nm High Performance 64Gb MLC NAND Flash Memory with 400MB/s Asynchronous Toggle DDR Interface**
		C. Kim, J. Ryu, T. Lee, H. Kim, J. Lim, J. Jeong, S. Seo, H. Jeon, B. Kim, I. Lee, D. Lee, P. Kwak, S. Cho, Y. Yim, C. Cho, W. Jeong, J.-M. Han, D. Song, K. Kyung, Y.-H. Lim and Y.-H. Jun
		Samsung Electronics, Korea
8:55	19-2	**A Fast Rewritable 90nm 512Mb NOR "B4-Flash" Memory with $8F^2$ Cell Size**
		T. Ogura, M. Mihara, Y. Kawajiri, K. Kobayashi, T. Sakaniwa, K. Nishikawa, S. Shimizu, S. Shukuri, N. Ajika and M. Nakashima
		GENUSION, Inc., Japan
9:20	19-3	***4-Times Faster* Rising V_{PASS}(10V), *15% Lower* Power V_{PGM} (20V), Wide Output Voltage Range Voltage Generator System for *4-Times Faster* 3D-Integrated Solid-State Drives**
		T. Hatanaka and K. Takeuchi
		The University of Tokyo, Japan

9:45	19-4	**A 512Mb Phase-Change Memory (PCM) in 90nm CMOS Achieving 2b/cell**
		G.F. Close*, U. Frey*,****, J. Morrish**, R. Jordan**, S. Lewis**, T. Maffitt**, M. Breitwisch***, C. Hagleitner*, C. Lam*** and E. Eleftheriou*
		**IBM Research Zurich, Switzerland, **IBM Essex Junction, ***IBM T. J. Watson Research Center, USA and ****RIKEN, Japan*

(Break 10:10-10:30)

Session 20		**High Speed and Low Power Receiver Techniques [Suzaku III]**
Chairpersons		S. Mutoh, *NTT Corp.* A. Emami, *CalTech*
8:30	20-1	**A 20-Gb/s, 0.66-pJ/bit Serial Receiver with 2-Stage Continuous-Time Linear Equalizer and 1-Tap Decision Feedback Equalizer in 45nm SOI CMOS**
		J.E. Proesel and T.O. Dickson
		IBM T. J. Watson Research Center, USA
8:55	20-2	**A 40Gb/s Adaptive Receiver with Linear Equalizer and Merged DFE/CDR**
		C.-L. Hsieh and S.-I. Liu
		National Taiwan University, Taiwan
9:20	20-3	**A 2.6mW/Gbps 12.5Gbps RX with 8-Tap Switched-Cap DFE in 32nm CMOS**
		T. Toifl*, C. Menolfi*, M. Ruegg**, R. Reutemann**, A. Prati**, D. Gardellini**, M. Brändli*, M. Kossel*, P. Buchmann*, P.A. Francese* and T. Morf*
		**IBM Research GmbH and **Miromico, Switzerland*
9:45	20-4	**A 4.4uW Wake-Up Receiver Using Ultrasound Data Communications**
		K. Yadav, I. Kymissis and P.R. Kinget
		Columbia University, USA

(Break 10:10-10:30)

Session 21		**Device-Based Circuit Techniques [Suzaku I]**
Chairpersons		K. Kobayashi, *Kyoto Institute of Technology* G. Lehmann, *Infineon Technologies AG*
10:30	21-1	**A True Random Number Generator Using Time-Dependent Dielectric Breakdown**
		N. Liu, N. Pinckney, S. Hanson, D. Sylvester and D. Blaauw
		University of Michigan, USA
10:55	21-2	**On-Chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS**
		S. Realov and K.L. Shepard
		Columbia University, USA
11:20	21-3	**Electrical Monitoring of Gate and Active Area Mask Misalignment Error**
		A. Bansal*, A. Singhee*, E. Acar* and G. Costrini**
		**IBM T. J. Watson Research Center and **IBM Systems & Technology Group, USA*

11:45	21-4	**A 80kS/s 36µW Resistor-Based Temperature Sensor Using BGR-Free SAR ADC with a Unevenly-Weighted Resistor String in 0.18µm CMOS**
		C.-K. Wu, W.-S. Chan and T.-H. Lin
		National Taiwan University, Taiwan
12:10	21-5	**PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability**
		J.-J. Kim*, R.M. Rao*, J. Schaub**, A. Ghosh**, A. Bansal*, K. Zhao***, B.P. Linder* and J. Stathis*
		**IBM T. J. Watson Research Center, **IBM Austin Research Lab and ***IBM SRDC, USA*

(Lunch 12:35-13:55)

Session 22		**DRAM and Memory Interfaces [Suzaku II]**
Chairpersons		R. Takemura, *Hitachi, Ltd.* J. Zerbe, *Rambus*
10:30	22-1	**3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype**
		J. Golz, J. Safran, B. He, D. Leu, M. Yin, T. Weaver, A. Vehabovic, Y. Sun, A. Cestero, B. Himmel, G. Maier, C. Kothandaraman, D. Fainstein, J. Barth, N. Robson, T. Kirihata, K. Rim and S. Iyer
		IBM Systems and Technology Group, USA
10:55	22-2	**In-Substrate-Bitline Sense Amplifier with Array-Noise- Gating Scheme for Low-Noise $4F^2$ DRAM Array Operable at 10-fF Cell Capacitance**
		Y. Yanagawa, T. Sekiguchi, A. Kotabe, K. Ono and R. Takemura
		Hitachi, Ltd., Japan
11:20	22-3	**A 12.8-Gb/s/Link Tri-Modal Single-Ended Memory Interface for Graphics Applications**
		A. Amirkhany, J. Wei, N. Mishra, J. Shen, W. Beyene, T. Chin, C. Huang, V. Gadde, K. Kaviani, P. Le, Mahabaleshwara, C. Madden, S. Mukherjee, L. Raghavan, K. Saito, D. Secker, F. Shuaeb, S. Srinivas, T. Wu, C. Tran, A. Vaidyanathan, K. Vyas, M. Jain, K. Chang and C. Yuan
		Rambus Inc., USA
11:45	22-4	**A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface**
		K. Kaviani, T. Wu, A. Amirkhany, J. Wei, J. Shen, C. Chen, T. Chin, W. Beyene, D. Dressler, V. Gadde, C. Huang, P. Le, Mahabaleshwara, C. Madden, N. Mishra, L. Raghavan, K. Saito, D. Secker, X. Shi, F. Shuaeb, S. Srinivas, C. Tran, A. Vaidyanath, K. Vyas, M. Jain, K. Chang and C. Yuan
		Rambus Inc., USA

(Lunch 12:35-13:55)

Session 23		**Power Management for Energy Harvesting [Suzaku III]**
Chairpersons		M. Takamiya, *The Univ. of Tokyo* B. Nikolic, *Univ of California, Berkeley*
10:30	23-1	**Platform Architecture for Solar, Thermal and Vibration Energy Combining with MPPT and Single Inductor**
		S. Bandyopadhyay and A.P. Chandrakasan
		Massachusetts Institute of Technology, USA

10:55	23-2	**A Reconfigurable SITITO Boost/Buck Regulator with Sub-Threshold Cross-Regulation-Free Dual-Mode Control for Energy-Harvesting Applications**
		M. Du, H. Lee and J. Liu
		University of Texas at Dallas, USA
11:20	23-3	**A Battery-Free 225 nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control**
		C.-Y. Hsieh*, Y.-H. Lee*, Y.-Y. Yang*, T.-C. Huang*, K.-H. Chen*, C.-C. Huang** and Y.-H. Lin**
		*National Chiao Tung University and **Realtek Semiconductor Corp., Taiwan*
11:45	23-4	**A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications**
		M. Lüders*, B. Eversmann**, J. Gerber**, K. Huber**, R. Kuhn**, D. Schmitt-Landsiedel* and R. Brederlow**
		*Munich University of Technology and **Texas Instruments, Germany*
12:10	23-5	**A 13.56MHz CMOS Rectifier with Switched-Offset for Reversion Current Control**
		Y. Lu*, W.-H. Ki* and J. Yi**
		*HKUST and **Texas Instruments, China*

(Lunch 12:35-13:55)

Session 24		**Digital Processors [Suzaku I]**
Chairpersons		H. Kabuo, *Panasonic Corp.* K. Wilcox, *AMD*
13:55	24-1	**A 45nm 48-Core IA Processor with Variation-Aware Scheduling and Optimal Core Mapping**
		S. Dighe*, S. Gupta**, V. De*, S. Vangal*, N. Borkar*, S. Borkar* and K. Roy**
		*Intel Corporation and **Purdue University, USA*
14:20	24-2	**A 75µW, 16-Channel Neural Spike-Sorting Processor with Unsupervised Clustering**
		V. Karkare, S. Gibson, C.-H. Yang, H. Chen and D. Marković
		University of California, Los Angeles, USA
14:45	24-3	**A 7.4mW 200MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios**
		T.-H. Yu, C.-H. Yang, D. Čabrić and D. Marković
		University of California, Los Angeles, USA
15:10	24-4	**Fully Integrated CMOS SoC for 3D Blu-Ray Player Applications**
		C.-C. Ju, T.-M. Liu, S.-H. Lin, C.-C. Yang, T.-H. Wei, H. Lin, C.C. Chiou, C. Tsai, T. Lin, R. Su, A. Lin, M.N. Tsou, J. Lee, S.H. Tai, C.-M. Wang, C.-C. Chen, H.-M. Lin, C.-Y. Cheng, F. Chiu, Y.-C. Chang, P.H. Liu, C.C. Yu, E. Tsai, Y.C. Fang, K. Peng, J.-B. Yang, D.-P. Liu, K.-H. Chen, B.-W. Hsieh, Y.-C. Lien, W.H. Tu, C.H. Chou, T.H. Kang, L.-C. Wang, T.C. Hsiao, V. Lin, H. Hsieh, C.-S. Wu and J. Chen
		Mediatek Inc., Taiwan
15:35	24-5	**A 52mW Full HD 160-Degree Object Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications**
		Y.-C. Su, K.-Y. Huang, T.-W. Chen, Y.-M. Tsai, S.-Y. Chien and L.-G. Chen
		National Taiwan University, Taiwan

(Break 16:00-16:15)

Session 25		Emerging ADCs [Suzaku II]
Chairpersons		M. Yoshioka, *FUJITSU LABORATORIES LTD.* I. Fujimori, *Broadcom Corp.*
13:55	25-1	**A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with Tri-Level Comparator in 40nm CMOS**
		A. Shikata, R. Sekimoto, T. Kuroda and H. Ishikuro
		Keio University, Japan
14:20	25-2	**A 1-V, 8b, 40MS/s, 113µW Charge-Recycling SAR ADC with a 14µW Asynchronous Controller**
		J.-H. Tsai, Y.-J. Chen, M.-H. Shen and P.-C. Huang
		National Tsing Hua University, Taiwan
14:45	25-3	**Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells**
		S. Weaver*, B. Hershberg** and U.-K. Moon**
		**Intel Corporation and **Oregon State University, USA*
15:10	25-4	**A Reconfigurable 1GSps to 250MSps, 7-bit to 9-bit Highly Time-Interleaved Counter ADC in 0.13µm CMOS**
		S. Danesh*,**, J. Hurwitz**, K. Findlater**, D. Renshaw* and R. Henderson*
		**Edinburgh University and **Gigle Networks, UK*
15:35	25-5	**A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation**
		S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar and P.K. Hanumolu
		Oregon State University Corvallis, USA

(Break 16:00-16:15)

Session 26		Power Management Technique [Suzaku III]
Chairpersons		K. Nose, *Renesas Electronics Corp.* G. Van der Plas, *IMEC*
13:55	26-1	**Dual-Loop System of Distributed Microregulators with High DC Accuracy, Load Response Time Below 500ps, and 85mV Dropout Voltage**
		Z. Toprak-Deniz*, J. Bulzacchelli*, T. Rasmus**, J. Iadanza**, W. Bucossi**, S. Kim*, R. Blanco**, C. Cox**, M. Chhabra**, C. Leblanc**, C. Trudeau** and D. Friedman*
		**IBM T. J. Watson Research Center and **IBM Systems and Technology Group, USA*
14:20	26-2	**MEMS-Switch-Based Power Management with Zero-Power Voltage Monitoring for Energy Accumulation Architecture on Dust-Size Wireless Sensor Nodes**
		T. Shimamura, M. Ugajin, K. Kuwabara, K. Takagahara, K. Suzuki, H. Morimura, M. Harada and S. Mutoh
		NTT Microsystem Integration Laboratories, Japan
14:45	26-3	**A 210 nW 29.3 ppm/°C 0.7 V Voltage Reference with a Temperature Range of -50 to 130°C in 0.13 µm CMOS**
		J. Lee and S.H. Cho
		KAIST, Korea

15:10	26-4	**A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1-V Input Switched-Capacitor 1/2 Voltage Converter with Output Voltage Trimming by Hot Carrier Injection and Periodic Activation Scheme**
		X. Zhang*, Y. Pu*, K. Ishida*, Y. Ryu**, Y. Okuma**, P.-H. Chen*, K. Watanabe**, T. Sakurai* and M. Takamiya*
		**The University of Tokyo and **Semiconductor Technology Academic Research Center (STARC), Japan*
15:35	26-5	**A Fast-Transient DVS-Capable Switching Converter with ΔI_L-Emulated Hysteretic Control**
		H. Chen and D. Ma
		The University of Texas at Dallas, USA

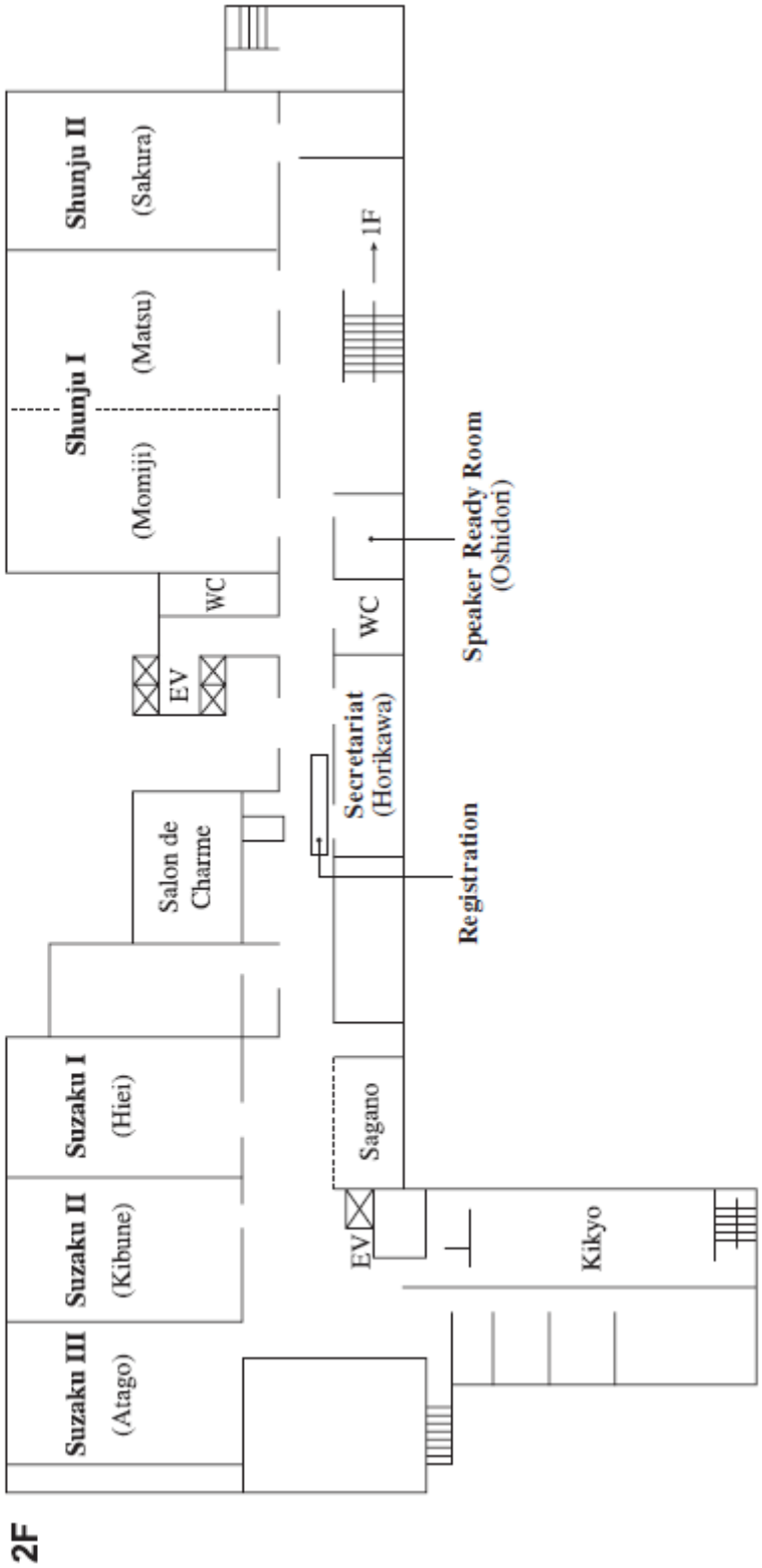
(Break 16:00-16:15)

Session 27		**Signal Processing for Wireline [Suzaku I]**
Chairpersons		R. Kuppuswamy, *Intel India* J. Gealow, *MediaTek Wireless, Inc.*
16:15	27-1	**A Laser Ranging Radar Transceiver with Modulated Evaluation Clock in 65nm CMOS Technology**
		W.-L. Lee, K.-C. Wu, J.-Y. Jiang and J. Lee
		National Taiwan University, Taiwan
16:40	27-2	**10Gb/s Serial I/O Receiver Based on Variable Reference ADC**
		E.-H. Chen, R. Yousry, T. Ali and C.-K.K. Yang
		University of California, Los Angeles, USA
17:05	27-3	**10 Gbps, 530 fJ/b Optical Transceiver Circuits in 40 nm CMOS**
		F. Liu*, D. Patil***, J. Lexau*, P. Amberg*, M. Dayringer*, J. Gainsley*, H.F. Moghadam*, X. Zheng*, J.E. Cunningham*, A.V. Krishnamoorthy*, E. Alon** and R. Ho*
		**Oracle Labs, **University of California, Berkeley and ***Rambus, USA*
17:30	27-4	**A Direct Sampling Multi-Channel Receiver for DOCSIS 3.0 in 65nm CMOS**
		E. Janssen*, K. Doris*, A. Zanikopoulos*, G. van der Weide*, M. Vertregt*, O. Jamin**, F. Courtois**, N. Blard**, M. Kristen**, S. Bertrand**, F. Riviere**, F. Deforeit**, G. Blanc**, Y. Penning**, F. Lefebvre**, D. Viguier**, M. Dubois**, V. Vrignaud**, C. Cazettes**, L. Schaller** and G. Jenvrin**
		**NXP Semiconductors, Eindhoven, The Netherlands and **NXP Semiconductors, Caen, France*

Session 28		**Nonvolatile Memory Applications [Suzaku II]**
Chairpersons		H. Yamauchi, *Fukuoka Institute of Technology* O. Jungroth, *Intel Corp.*
16:15	28-1	**A 45nm 1Mb Embedded STT-MRAM with Design Techniques to Minimize Read-Disturbance**
		J.P. Kim, T. Kim, W. Hao, H.M. Rao, K. Lee, X. Zhu, X. Li, W. Hsu, S.H. Kang, N. Matt and N. Yu
		Qualcomm Incorporated, USA

16:40	28-2	**Fully Parallel 6T-2MTJ Nonvolatile TCAM with Single-Transistor-Based Self Match-Line Discharge Control**
		S. Matsunaga*, A. Katsumata*, M. Natsui*, S. Fukami**, T. Endoh*, H. Ohno* and T. Hanyu*
		**Tohoku University and **NEC Corporation, Japan*
17:05	28-3	**A Content Addressable Memory Using Magnetic Domain Wall Motion Cells**
		R. Nebashi*, N. Sakimura*, Y. Tsuji*, S. Fukami*, H. Honjo*, S. Saito*, S. Miura*, N. Ishiwata*, K. Kinoshita*, T. Hanyu**, T. Endoh**, N. Kasai**, H. Ohno** and T. Sugibayashi*
		**NEC Corporation and **Tohoku University, Japan*
17:30	28-4	**A Non-volatile Look-Up Table Design Using PCM (Phase-Change Memory) Cells**
		C.-Y. Wen*, J. Li**, S. Kim**, M. Breitwisch**, C. Lam**, J. Paramesh* and L.T. Pileggi*
		**Carnegie Mellon University and **IBM T. J. Watson Research Center, USA*

FLOOR MAP


2F
Suzaku III (Atago)
Suzaku II (Kibune)
Suzaku I (Hiei)
Salon de Charme
Shunju I (Momiji)
Shunju I (Matsu)
Shunju II (Sakura)
WC
EV
EV
Sagano
Secretariat (Horikawa)
WC
Registration
Speaker Ready Room (Oshidori)
Kikyo
1F