2012 Symposium on VLSI Circuits Accepted Papers Listed by Submission Number

The Titles and Author List appear as they were submitted by the author.
They will be proofed and corrected for the Proceedings and Final Program.

Submission Number: **5**
Session/Paper Slot Number: **C5-1**
Wednesday, June 13 - 1:30pm
A 440pJ/bit 1Mb/s 2.4GHz Multi-Channel FBAR-based TX and an Integrated Pulse-shaping PA, Arun Paidimarri, Phillip Nadeau, Patrick Mercier and Anantha Chandrakasan

Submission Number: **11**
Session/Paper Slot Number: **C20-3**
Friday, June 15 - 2:20pm
A Standard Cell Compatible Bidirectional Repeater with Thyristor Assist, Sudhir Satpathy, Dennis Sylvester and David Blaauw

Submission Number: **13**
Session/Paper Slot Number: **C23-2**
Friday, June 15 - 3:50pm
A Fully Electrical Startup Batteryless Boost Converter with 50mV Input Voltage for Thermoelectric Energy Harvesting, Hao-Yen Tang, Po-Shuan Weng, Po-Chih Ku and Liang-Hung Lu

Submission Number: **14**
Session/Paper Slot Number: **C3-1**
Wednesday, June 13 - 10:25am
Circuit Techniques to Overcome Class–D Audio Amplifier Limitations in Mobile Devices, Xicheng Jiang, Jungwoo Song, Minsheng Wang, Jianlong Chen, Sasi Kumar Arunachalam and Todd Brooks

Submission Number: **15**
Session/Paper Slot Number: **C5-2**
Wednesday, June 13 - 1:55pm
An 8-PPM, 45 pJ/bit UWB transmitter with reduced number of PA elements, Vahid Majidzadeh, Alexandre Schmid, Yusuf Leblebici and Jan Rabaey

Submission Number: **17**
Session/Paper Slot Number: **C9-1**
Thursday, June 14 - 8:05am
A 0.6V 2.9μW Mixed-Signal Front-End for ECG Monitoring, Marcus Yip, Jose L. Bohorquez and Anantha P. Chandrakasan

Submission Number: **25**
Session/Paper Slot Number: **J-C12-4**
Thursday, June 14 - 2:45pm
A 47% Access Time Reduction with a Worst-Case Timing-Generation Scheme Utilizing a Statistical Method for Ultra Low Voltage SRAMs, Atsushi Kawasumi, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Fumihiko Tachibana, Yusuke Niki, Sinichi Sasaki and Tomoaki Yabe

Submission Number: **31**
Session/Paper Slot Number: **C18-1**
Friday, June 15 - 10:00am
A Low Power Many-Core SoC with Two 32-Core Clusters Connected by Tree based NoC for Multimedia Applications, Xu Hui, Tanabe Jun, Usui Hiroyuki, Hosoda Soichiro, Sano Toru, Yamamoto Kazumasa, Kodaka Takeshi, Nonogaki Nobuhiro, Ozaki Nau and Miyamori Takashi

Submission Number: **33**
Session/Paper Slot Number: **C11-2**
Thursday, June 14 - 10:25am
A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure, Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U and Rui Martins

Submission Number: **34**
Session/Paper Slot Number: **C11-4**
Thursday, June 14 - 11:15am
A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC, Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U and Rui Martins

Submission Number: **39**
Session/Paper Slot Number: **C19-4**
Friday, June 15 - 11:15am
A Reconfigurable Mostly-Digital ΔΣ ADC with a Worst-Case FOM of 160dB, Gerry Taylor and Ian Galton

Submission Number: **51**
Session/Paper Slot Number: **C21-2**
Friday, June 15 - 1:55pm
High Area-Efficient DC-DC Converter using Time-Mode Miller Compensation (TMMC), Sung-Wan Hong, Tae-Hwang Kong, Seungchul Jung, Sung-Woo Lee, Se-Won Wang, Jong-Pil Im and Gyu-Hyeong Cho

Submission Number: **55**
Session/Paper Slot Number: **J-C12-2**
Thursday, June 14 - 1:55pm
Voltage Droop Reduction Using Throttling Controlled by Timing Margin Feedback, Michael Floyd, Alan Drake, Robert Berry, Harold Chase, Richard Willaman and Jarom Pena

Submission Number: **66**
Session/Paper Slot Number: **C4-2**
Wednesday, June 13 - 1:55pm
An Event-Driven, Alias-Free ADC with Signal-Dependent Resolution, Colin Weltin-Wu and Yannis Tsividis

Submission Number: **67**
Session/Paper Slot Number: **J-C14-2**
Thursday, June 14 - 3:50pm
A 260mV L-shaped 7T SRAM with Bit-Line (BL) Swing Expansion Schemes Based on Boosted BL, Asymmetric-VTH Read-Port, and Offset Cell VDD Biasing Techniques, Ming-Pin Chen, Lai-Fu Chen, Meng-Fan Chang, Shu-Meng Yang, Yao-Jen Kuo, Jui-Jen Wu, Mon-Shu Ho, Hsiu-Yun Su, Yuan-Hua Chu, Wen-Ching Wu, Tzu-Yi Yang and Hiroyuki Yamauchi

Submission Number: **68**
Session/Paper Slot Number: **J-T17-4**
Thursday, June 14 - 11:15am
Dynamic Intrinsic Chip ID Using 32nm High-K/Metal Gate SOI Embedded DRAM, Daniel Fainstein, Sami Rosenblatt, Alberto Cestero, Norman Robson, Toshiaki Kirihata and Subramanian S Iyer

Submission Number: **73**
Session/Paper Slot Number: **C11-1**
Thursday, June 14 - 10:00am
A 2.8GS/s 44.6mW Time-Interleaved ADC Achieving 50.9dB SNDR and 3dB Effective Resolution Bandwidth of 1.5GHz in 65nm CMOS, Dusan Stepanovic and Borivoje Nikolic

Submission Number: **88**
Session/Paper Slot Number: **C9-3**
Thursday, June 14 - 8:55am
A Wirelessly Powered Log-based Closed-loop Deep Brain Stimulation SoC with Two-way Wireless Telemetry for Treatment of Neurological Disorders, Hyo-Gyuem Rhew, Jaehun Jeong, Jeffrey Fredenburg, Sunjay Dodani, Parag Patil and Michael Flynn

Submission Number: **89**
Session/Paper Slot Number: **C4-1**
Wednesday, June 13 - 1:30pm
A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators, Yun-Shiang Shu

Submission Number: **94**
Session/Paper Slot Number: **C19-5**
Friday, June 15 - 11:40am
A 71dB Dynamic Range Third-Order $\Delta\Sigma$ TDC using Charge-Pump, Manideep Gande, Nima Maghari, Taehwan Oh and Un-Ku Moon

Submission Number: **98**
Session/Paper Slot Number: **C21-1**
Friday, June 15 - 1:30pm
A 50nA Quiescent Current Asynchronous Digital-LDO with PLL-Modulated Fast-DVS Power Management in 40nm CMOS for 5.6 times MIPS Performance, Yu-Huei Lee, Shen-Yu Peng, Chun-Hsien Wu, Chao-Chang Chiu, Yao-Yi Yang, Ming-Hsin Huang, Ke-Horng Chen, Ying-Hsi Lin, Shih-Wei Wang, Ching-Yuan Yeh, Chen-Chih Huang and Chao-Cheng Lee

Submission Number: **101**
Session/Paper Slot Number: **C23-1**
Friday, June 15 - 3:25pm
A 0.45-V Input On-Chip Gate Boosted (OGB) Buck Converter in 40-nm CMOS with More Than 90% Efficiency in Load Range from 2☐W to 50☐W, Xin Zhang, Po-Hung Chen, Yoshikatsu Ryu, Koichi Ishida, Yasuyuki Okuma, Kazunori Watanabe, Takayasu Sakurai and Makoto Takamiya

Submission Number: **102**
Session/Paper Slot Number: **C17-3**
Friday, June 15 - 8:55am
A Clock Jitter Reduction Circuit Using Gated Phase Blending Between Self-Delayed Clock Edges, Kiichi Niitsu, Naohiro Harigai, Daiki Hirabayashi, Daiki Oki, Masato Sakurai, Osamu Kobayashi, Takahiro J. Yamaguchi and Haruo Kobayashi

Submission Number: **104**
Session/Paper Slot Number: **C18-2**
Friday, June 15 - 10:25am
A 69mW 140-meter/60fps and 60-meter/300fps Intelligent Vision SoC for Versatile Automotive Applications, Yi-Min Tsai, Tien-Ju Yang, Chih-Chung Tsai, Keng-Yen Huang and Liang-Gee Chen

Submission Number: **106**
Session/Paper Slot Number: **C19-1**
Friday, June 15 - 10:00am
A 50 fJ/conv. Continuous Time delta-sigma Modulator with High-order Single Opamp Integrator using Optimization-based Design Method, Kazuo Matsukawa, Koji Obata, Yosuke Mitani and Shiro Dosho

Submission Number: **108**
Session/Paper Slot Number: **C11-5**
Thursday, June 14 - 11:40am
A 3.2fJ/c.-s. 0.35V 10b 100KS/s SAR ADC in 90nm CMOS, Hung-Yen Tai, Hung-Wei Chen and Hsin-Shu Chen

Submission Number: **113**
Session/Paper Slot Number: **C3-2**
Wednesday, June 13 - 10:50am
A 5.2mW, 0.0016% THD up to 20kHz, Ground-Referenced Audio Decoder with PSRR-enhanced Class-AB 16Ohm Headphone Amplifiers, Shon-Hang Wen and Cheng-Chung Yang

Submission Number: **114**
Session/Paper Slot Number: **C02-3**
Wednesday, June 13 - 11:15am
A 32.4 ppm/°C 3.2-1.6V Self-chopped Relaxation Oscillator with Adaptive Supply Generation, Keng-Jan Hsiao

Submission Number: **116**
Session/Paper Slot Number: **C15-5**
Thursday, June 14 - 5:05pm
An 88dB SNR, 30μm pixel pitch Infra-Red image sensor with a 2-step 16 bit A/D conversion, Arnaud Peizerat, Jean-Pierre Rostaing, Noureddine Zitouni, Nicolas Baier, Fabrice Guellec, Rémi Jalby and Michael Tchagaspanian

Submission Number: **117**
Session/Paper Slot Number: **C02-2**
Wednesday, June 13 - 10:50am
A 160-GHz Receiver-Based Phase-Locked Loop in 65 nm CMOS Technology, Wei-Zen Chen, Tai-You Lu, Yan-Ting Wang, Jhong-Ting Jian, Yi-Hung Yang, Guo-Wei Huang, Wen-De Liu, Chih-Hua Hsiao, Shu-Yu Lin and Jung Yen Liao

Submission Number: **118**
Session/Paper Slot Number: **C13-3**
Thursday, June 14 - 2:20pm
A 25-Gb/s 2.2-W Optical Transceiver Using an Analog FE Tolerant to Power Supply Noise and Redundant Data Format Conversion in 65-nm CMOS, Takashi Takemoto, Hiroki Yamashita, Takehito Kamimura, Fumio Yuki, Noboru Masuda, Hidehiro Toyoda, Norio Chujo, Kenji Kogo, Yong Lee, Shinji Tsuji and Shinji Nishimura

Submission Number: **121**
Session/Paper Slot Number: **C22-4**
Friday, June 15 - 4:40pm
A 7b, 3.75ps Resolution Two-Step Time-to-Digital Converter in 65nm CMOS Using Pulse-Train Time Amplifier, KwangSeok Kim, YoungHwa Kim, WonSik Yu and SeongHwan Cho

Submission Number: **126**
Session/Paper Slot Number: **C7-4**
Wednesday, June 13 - 4:40pm
A UWB IR Timed-Array Radar Using Time-Shifted Direct-Sampling Architecture, Chang-Ming Lai, Kai-Wen Tan, Liu-Yuan Yu, Yen-Ju Chen, Jun-Wei Huang, Shr-Chau Lai, Feng-Hsu Chung, Chia-Fung Yen, Jen-Ming Wu, Po-Chiun Huang, Keh-Jeng Chang, Shi-Yu Huang and Ta-Shun Chu

Submission Number: **128**
Session/Paper Slot Number: **C20-2**
Friday, June 15 - 1:55pm
A 3-stage Pseudo Single-phase Flip-flop Family, Hamid Partovi, Alfred Yeung, Luca Ravezzi and Mark Horowitz

Submission Number: **130**
Session/Paper Slot Number: **C13-2**
Thursday, June 14 - 1:55pm
A Wide Common-Mode Fully-Adaptive Multi-Standard 12.5Gb/s Backplane Transceiver in 28nm CMOS, Jafar Savoj, Kenny Hsieh, Parag Upadhyaya, Fu-Tai An, Ade Bekele, Stanley Chen, Xuewen Jiang, Kang Wei Lai, Chi Fung Poon, Aman Sewani, Didem Turker, Karthik Venna, Daniel Wu, Bruce Xu, Elad Alon and Ken Chang

Submission Number: **132**
Session/Paper Slot Number: **J-C8-4**
Thursday, June 14 - 9:20am
A 28nm High-k Metal-Gate SRAM with Asynchronous Cross-Couple Read Assist (AC2RA) Circuitry Achieving 3X Reduction on Speed Variation for Single Ended Arrays, Robin Lee, Jung-Ping Yang, Chia-En Huang, Chih-Chieh Chiu, Wei-Shuo Kao, Hong-Chen Cheng, Hong-Jen Liao and Jonathan Chang

Submission Number: **134**
Session/Paper Slot Number: **C10-1**
Thursday, June 14 - 10:00am
A -70dBm-Sensitivity 522Mbps 0.19nJ/bit-TX 0.43nJ/bit-RX Transceiver for TransferJet(TM) SoC in 65nm CMOS, Daisuke Miyashita, Kenichi Agawa, Hirotsugu Kajihara, Kenichi Sami, Masaomi Iwanaga, Yosuke Ogasawara, Tomohiko Ito, Daisuke Kurose, Naotaka Koide, Toru Hashimoto, Hiroki Sakurai, Takafumi Yamaji, Takashi Kurihara, Kazumi Sato, Ichiro Seto, Hiroshi Yoshid

Submission Number: **141**
Session/Paper Slot Number: **C11-3**
Thursday, June 14 - 10:50am
A 4.5-mW 8-b 750-MS/s 2-b/Step Asynchronous Subranged SAR ADC in 28-nm CMOS Technology, Yuan-Ching Lien

Submission Number: **142**
Session/Paper Slot Number: **C16-2**
Friday, June 15 - 8:30am
A New 3-bit Programming Algorithm using SLC-to-TLC Migration for 8MB/s High Performance TLC NAND Flash Memory, Seung-hwan Shin

Submission Number: **147**
Session/Paper Slot Number: **C18-4**
Friday, June 15 - 11:15am
A Sub-100μW Multi-Functional Cardiac Signal Processor for Mobile Healthcare Applications, Shu-Yu Hsu, Yingchieh Ho, Yuhwai Tseng, Ting-You Lin, Po-Yao Chang, Jen-Wei Lee, Ju-Hung Hsiao, Siou-Ming Chuang, Tze-Zheng Yang, Po-Chun Liu, Ten-Fang Yang, Ray-Jade Chen, Chauchin Su and Chen-Yi Lee

Submission Number: **149**
Session/Paper Slot Number: **C22-1**
Friday, June 15 - 3:25pm
Design of a 2.5-GHz, 3-ps Jitter, 8-Locking-Cycle, All-Digital Delay-Locked Loop with Cycle-by-Cycle Phase Adjustment, Chun-Yuan Cheng, Jinn-Shyan Wang, Cheng-Tai Yeh and Jenn-Shyan Sheu

Submission Number: **153**
Session/Paper Slot Number: **J-C8-1**
Thursday, June 14 - 8:05am
A 0.41μA Standby Leakage 32Kb Embedded SRAM with Low-Voltage Resume-Standby utilizing All Digital Current Comparator in 28nm HKMG CMOS, Noriaki Maeda, Shigenobu Komatsu, Masao Morimoto and Yasuhisa Shimazaki

Submission Number: **157**
Session/Paper Slot Number: **C20-1**
Friday, June 15 - 1:30pm
A Shorted Global Clock Design for Multi-GHz 3D Stacked Chips, Liang-Teck Pang, Phillip Restle, Mathew Wordeman, Joel Silberman, Robert Franch and Gary Maier

Submission Number: **169**
Session/Paper Slot Number: **C3-4**
Wednesday, June 13 - 11:40am
A 1.2V 8.3nJ Energy-Efficient CMOS Humidity Sensor for RFID Applications, Zhichao Tan, Youngcheol Chae, Roel Daamen, Aurélie Humbert, Youri Ponomarev and Michiel Pertijs

Submission Number: **171**
Session/Paper Slot Number: **J-C12-1**
Thursday, June 14 - 1:30pm
A 22nm Dynamically Adaptive Clock Distribution for Voltage Droop Tolerance, Keith Bowman, Carlos Tokunaga, Tanay Karnik, Vivek De and Jim Tschanz

Submission Number: **172**
Session/Paper Slot Number: **C10-5**
Thursday, June 14 - 11:40am
A 13.5mA Sub-2.5dB NF Multi-Band Receiver, Mohyee Mikhemar, Ahmad Mirzaei, Amir Hadji-Abdolhamid, Janice Chiu and Hooman Darabi

Submission Number: **175**
Session/Paper Slot Number: **C19-3**
Friday, June 15 - 10:50am
An 85dB SFDR 67dB SNDR 8OSR 240MS/s Sigma-Delta ADC with Nonlinear Memory Error Calibration, Seung-Chul Lee, Brian Elies and Yun Chiu

Submission Number: **179**
Session/Paper Slot Number: **J-C8-3**
Thursday, June 14 - 8:55am
A SRAM Cell Array with Adaptive Leakage Reduction Scheme for Data Retention in 28nm High-K Metal-Gate CMOS, Peter Hsu, Yukit Tang, Derek Tao, Ming-Chieh Huang, Min-Jer Wang, CH Wu and Quincy Li

Submission Number: **180**
Session/Paper Slot Number: **C16-4**
Friday, June 15 - 9:20am
Adaptive Multi-Pulse Program Scheme Based on Tunneling Speed Classification for Next Generation Multi-Bit/Cell NAND FLASH, Yong Sung Cho, Il Han Park, Sang Young Yoon, Nam Hee Lee, Sang Hyun Joo, Ki-Whan Song, Kihwan Choi, Jin Man Han, Kye Hyun Kyung and Young-Hyun Jun

Submission Number: **186**
Session/Paper Slot Number: **C02-1**
Wednesday, June 13 - 10:25am
Components for Generating and Phase Locking 390-GHz Signal in 45-nm CMOS, Dongha Shim, Dimitrios Koukis, Daniel Arenas, David Tanner, Eunyoung Seok, Joe Brewer and Kenneth O

Submission Number: **193**
Session/Paper Slot Number: **C13-1**
Thursday, June 14 - 1:30pm
ulpq30, Thomas Toifl, Michael Ruegg, Rajesh Inti, Christian Menolfi, Matthias Braendli, Marcel Kossel, Peter Buchmann, Pier Andrea Francese and Thomas Morf

Submission Number: **195**
Session/Paper Slot Number: **J-C14-5**
Thursday, June 14 - 5:05pm
A 2.8GHz 128-entry x 152b 3-Read/2-Write Multi-Precision Floating-Point Register File and Shuffler in 32nm CMOS, Steven Hsu, Amit Agarwal, Mark Anders, Himanshu Kaul, Sanu Mathew, Farhana Sheikh, Ram Krishnamurthy and Shekhar Borkar

Submission Number: **202**
Session/Paper Slot Number: **J-C14-4**
Thursday, June 14 - 4:40pm
1Gsearch/sec Ternary Content Addressable Memory Compiler with Silicon-Aware Early-Predict Late-Correct Single-Ended Sensing, Igor Arsovski, Travis Hebig, Daniel Dobson and Reid Wistort

Submission Number: **203**
Session/Paper Slot Number: **J-C6-1**
Wednesday, June 13 - 3:25pm
A 0.13µm 8Mb Logic Based CuxSiyO Resistive Memory with Self-Adaptive Yield Enhancement and Operation Power Reduction, X. Y. Xue, W. X. Jian, J. G. Yang, F. J. Xiao, G. Chen, X. L. Xu, Y. F. Xie, Y. Y. Lin, R. Huang, Q. T. Zhou and J. G. Wu

Submission Number: **206**
Session/Paper Slot Number: **C21-4**
Friday, June 15 - 2:45pm
A 198-ns/V VO-Hopping Reconfigurable RGB LED Driver with Automatic ΔVO Detection and Quasi-Constant-Frequency Predictive Peak Current Control, Yi Zhang, Hai Chen and Dongsheng Ma

Submission Number: **211**
Session/Paper Slot Number: **C5-4**
Wednesday, June 13 - 2:45pm
A 2.4GHz Hybrid PPF Based BFSK Receiver with ±180ppm Frequency Offset Tolerance for Wireless Sensor Networks, Ronghua Ni, Kartikeya Mayaram and Terri Fiez

Submission Number: **213**
Session/Paper Slot Number: **J-C6-3**
Wednesday, June 13 - 4:15pm
1Mb 4T-2MTJ Nonvolatile STT-RAM for Embedded Memories Using 32b Fine-Grained Power Gating Technique with 1.0ns/200ps Wake-up/Power-off Times, Takashi Ohsawa, Hiroki Koike, Sadahiko Miura, Hiroaki Honjo, Keiichi Tokutome, Shoji Ikeda, Takahiro Hanyu, Hideo Ohno and Tetsuo Endoh

Submission Number: **215**
Session/Paper Slot Number: **C16-3**
Friday, June 15 - 8:55am
x11 Performance Increase, x6.9 Endurance Enhancement, 93% Energy Reduction of 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSDs by Data Fragmentation Suppression, Hiroki Fujii, Kousuke Miyaji, Koh Johguchi, Kazuhide Higuchi, Chao Sun and Ken Takeuchi

Submission Number: **220**
Session/Paper Slot Number: **C16-1**
Friday, June 15 - 8:05am
A Logic-Compatible Embedded Flash Memory Featuring a Multi-Story High Voltage Switch and a Selective Refresh Scheme, Seung-Hwan Song, Ki Chul Chun and Chris H. Kim

Submission Number: **221**
Session/Paper Slot Number: **C9-2**
Thursday, June 14 - 8:30am
A 700µW 8-Channel EEG/Contact-impedance Acquisition System for Dry-electrodes, Srinjoy Mitra, Jiawei Xu, Akinori Matsumoto, Kofi A. A. Makinwa, Chris Van Hoof and Firat Yazicioglu Refet

Submission Number: **222**
Session/Paper Slot Number: **C17-4**
Friday, June 15 - 9:20am
A 1.22mW/Gb/s 9.6Gb/s Data Jitter Mixing Forwarded-Clock Receiver Robust against Power Noise with 1.92ns Latency Mismatch between Data and Clock in 65nm CMOS, Sang-Hye Chung and Lee-Sup Kim

Submission Number: **232**
Session/Paper Slot Number: **C15-4**
Thursday, June 14 - 4:40pm
A Fully-Electronic Charge-Based DNA Sequencing CMOS Biochip, Arun Manickam, Ritruaj Singh, Nicholas Wood, Bingling Li, Andrew Ellington and Arjang Hassibi

Submission Number: **236**
Session/Paper Slot Number: **C3-3**
Wednesday, June 13 - 11:15am
A Sub-1V 3.9µW Bandgap Reference with a 3σ Inaccuracy of ±0.34% from −50°C to +150°C using Piecewise-Linear-Current Curvature Compensation, Shinya Sano, Yasuhiko Takahashi, Masashi Horiguchi and Moriyoshi Ota

Submission Number: **239**
Session/Paper Slot Number: **C17-1**
Friday, June 15 - 8:05am
A 25-Gb/s 5-mW CMOS CDR/Deserializer, Jun Won Jung and Behzad Razavi

Submission Number: **243**
Session/Paper Slot Number: **C4-3**
Wednesday, June 13 - 2:20pm
A 10-Bit 1-GHz 33-mW CMOS ADC, Bibhu Datta Sahoo and Behzad Razavi

Submission Number: **245**
Session/Paper Slot Number: **C15-2**
Thursday, June 14 - 3:50pm
Nanostructured CMOS Wireless Ultra-Wideband Label-free DNA Analysis SoC, hamed mazhab jafari, Leyla Soleymani, Karim Abdelhalim, Edward Sargent, Shanna Kelley and Roman Genov

Submission Number: **251**
Session/Paper Slot Number: **C10-4**
Thursday, June 14 - 11:15am
A Harmonic-Rejecting CMOS LNA for Broadband Radios, Joung Won Park and Behzad Razavi

Submission Number: **252**
Session/Paper Slot Number: **C13-4**
Thursday, June 14 - 2:45pm
A 100+ meter 12Gb/s/Lane Copper Cable Link Based on Clock-Forwarding, Tamer Ali, Won Ho Park, Preeti Mulage, E-Hung Chen, Ron Ho and Chih-Kong Ken Yang

Submission Number: **253**
Session/Paper Slot Number: **C18-5**
Friday, June 15 - 11:40am
A 0.25V 460nW Asynchronous Neural Signal Processor with Inherent Leakage Suppression, Tsung-Te Liu and Jan Rabaey

Submission Number: **254**
Session/Paper Slot Number: **C10-3**
Thursday, June 14 - 10:50am
A +30.5 dBm CMOS Doherty Power Amplifier with Reliability Enhancement Technique, Kohei Onizuka, Shigehito Saigusa and Shoji Otaka

Submission Number: **259**
Session/Paper Slot Number: **C02-4**
Wednesday, June 13 - 11:40am
A 280nW, 100kHz, 1-Cycle Start-up Time, On-chip CMOS Relaxation Oscillator Employing a Feedforward Period Control Scheme, Takashi Tokairin, Koichi Nose, Koichi Takeda, Koichiro Noguchi, Tadashi Maeda, Kazuyoshi Kawai and Masayuki Mizuno

Submission Number: **264**
Session/Paper Slot Number: **C23-4**
Friday, June 15 - 4:40pm
A 2.98nW Bandgap Voltage Reference Using a Self-Tuning Low Leakage Sample and Hold, Yen-Po Chen, Matt Fojtik, David Blaauw and Dennis Sylvester

Submission Number: **280**
Session/Paper Slot Number: **J-C8-2**
Thursday, June 14 - 8:30am
A 13.8pJ/Access/Mbit SRAM with Charge Collector Circuits for Effective Use of Non-Selected Bit Line Charges, Shinichi Moriwaki, Atsushi Kawasumi, Yasue Yamamoto, Shinji Miyano, Hirofumi Shinohara, Toshikazu Suzuki and Takayasu Sakurai

Submission Number: **292**
Session/Paper Slot Number: **C18-3**
Friday, June 15 - 10:50am
A 4320p 60fps H.264/AVC Intra-Frame Encoder Chip with 1.41Gbins/s CABAC, Dajiang Zhou, Gang He, Wei Fei, Zhixiang Chen, Jinjia Zhou and Satoshi Goto

Submission Number: **304**
Session/Paper Slot Number: **C23-3**
Friday, June 15 - 4:15pm
Integrated All-silicon Thin-film Power Electronics on Flexible Sheets For Ubiquitous Wireless Charging Stations based on Solar-energy Harvesting, Liechao Huang, Warren Rieutort-Louis, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm and Naveen Verma

Submission Number: **310**
Session/Paper Slot Number: **C17-2**
Friday, June 15 - 8:30am
4×12 Gb/s 0.96 pJ/b/lane Analog-IIR Crosstalk Cancellation and Signal Reutilization Receiver for Single-Ended I/Os in 65 nm CMOS, Taehyoun Oh and Ramesh Harjani

Submission Number: **322**
Session/Paper Slot Number: **C15-1**
Thursday, June 14 - 3:25pm
High-resolution Sensing Sheet for Structural-health Monitoring via Scalable Interfacing of Flexible Electronics with High-performance ICs, Yingzhe Hu, Warren Rieutort-Louis, Josue Sanz-Robinson, Katherine Song, James C. Sturm, Sigurd Wagner and Naveen Verma

Submission Number: **325**
Session/Paper Slot Number: **C23-5**
Friday, June 15 - 5:05pm
A 635pW Battery Voltage Supervisory Circuit for Miniature Sensor Nodes, Inhee Lee, Suyoung Bang, Yoonmyung Lee, Yejoong Kim, Gyouho Kim, Dennis Sylvester and David Blaauw

Submission Number: **326**
Session/Paper Slot Number: **C15-3**
Thursday, June 14 - 4:15pm
A Fully Integrated Hepatitis B Virus (HBV) DNA Detection SoC based on Monolithic Polysilicon Nanowire CMOS Process, Che-Wei Huang, Yu-Jie Huang, Pei-Wen Yen, Hsiao-Ting Hsueh, Chia-Yi Lin, Min-Cheng Chen, Chia-Hua Ho, Fu-Liang Yang, Hann-Huei Tsai, Hsin-Hao Liao, Ying-Zong Juang, Chorng-Kuang Wang, Chih-Ting Lin and Shey-Shi Lu

Submission Number: **335**
Session/Paper Slot Number: **C5-3**
Wednesday, June 13 - 2:20pm
An All 0.5V, 1Mbps, 315MHz OOK Transceiver with 38-uW Career-Frequency-Free Intermittent Sampling Receiver and 52-uW Class-F Transmitter in 40-nm CMOS, Akira Saito, Kentaro Honda, Yunfei Zheng, Shunta Iguchi, Kazunori Watanabe, Takayasu Sakurai and Makoto Takamiya

Submission Number: **338**
Session/Paper Slot Number: **J-T17-5**
Thursday, June 14 - 11:40am
A Fully-Digital Phase-Locked Low Dropout Regulator in 32nm CMOS, Arijit Raychowdhury, Dinesh Somasekhar, James Tschanz and Vivek De

Submission Number: **339**
Session/Paper Slot Number: **C20-4**
Friday, June 15 - 2:45pm
An integral path self-calibration scheme for a 20.1-26.7GHz dual-loop PLL in 32nm SOI CMOS, Mark Ferriss, Jean-Olivier Plouchart, Arun Natarajan, Alexander Rylyakov, Benjamin Parker, Aydin Babakhani, Soner Yaldiz, Bodhisatwa Sadhu, Alberto Valdes-Garcia, Jose Tierno and Daniel Friedman

Submission Number: **341**
Session/Paper Slot Number: **C22-3**
Friday, June 15 - 4:15pm
A 61-dB SNDR 700 µm2 Second-Order All-Digital TDC with Low-Jitter Frequency Shift Oscillators and Dynamic Flipflops, Toshihiro Konishi, Keisuke Okuno, Shintaro Izumi, Masahiko Yoshimoto and Hiroshi Kawaguchi

Submission Number: **343**
Session/Paper Slot Number: **C7-3**
Wednesday, June 13 - 4:15pm
A 21.5mW 10+Gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS, Lingkai Kong and Elad Alon

Submission Number: **344**
Session/Paper Slot Number: **C4-4**
Wednesday, June 13 - 2:45pm
A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers, Benjamin Hershberg, Skyler Weaver, Kazuki Sobue, Seiji Takeuchi, Koichi Hamashita and Un-Ku Moon

Submission Number: **349**
Session/Paper Slot Number: **C9-4**
Thursday, June 14 - 9:20am
A Fully-Integrated 10.5µW Miniaturized (0.125µm2) Wireless Neural Sensor, Daniel Yeager, William Biederman, Nathan Narevsky, Elad Alon and Jan Rabaey

Submission Number: **351**
Session/Paper Slot Number: **C19-2**
Friday, June 15 - 10:25am
A 5MHz BW 70.7dB SNDR Noise-Shaped Two-Step Quantizer Based $\Delta\Sigma$ ADC, Taehwan Oh, Nima Maghari and Un-Ku Moon

Submission Number: **358**
Session/Paper Slot Number: **J-C14-1**
Thursday, June 14 - 3:25pm
Isolated Preset Architecture for a 32nm SOI embedded DRAM Macro, John Barth, Don Plass, Adis Vehabovic, Rajiv Joshi, Rouwaida Kanj, Steve Burns and Todd Weaver

Submission Number: **364**
Session/Paper Slot Number: **J-C12-3**
Thursday, June 14 - 2:20pm
An On-Die All-Digital Delay Measurement Circuit with 250fs Accuracy, Mozhgan Mansuri, Bryan Casper and Frank O'Mahony

Submission Number: **365**
Session/Paper Slot Number: **J-C14-3**
Thursday, June 14 - 4:15pm
A 1.6-mm2 38-mW 1.5-Gb/s LDPC Decoder Enabled by Refresh-Free Embedded DRAM, Youn Sung Park, David Blaauw, Dennis Sylvester and Zhengya Zhang

Submission Number: **370**
Session/Paper Slot Number: **C10-2**
Thursday, June 14 - 10:25am
A 2.4GHz WLAN Transceiver with Fully-integrated Highly-linear 1.8V 28.4dBm PA, 34dBm T/R Switch, 240MS/s DAC, 320MS/s ADC, and DPLL in 32nm SoC CMOS, Yulin Tan, Jon Duster, Chang-tsung Fu, Erkan Alpman, Ajay Balankutty, Chun C. Lee, Ashoke Ravi, Stefano Pellerano, Kailash Chandrashekar, Hyung Seok Kim, Brent Carlton, Satoshi Suzuki, Mohammed Shafi, Yorgos Palaskas and Hasnain Lakdawala

Submission Number: **376**
Session/Paper Slot Number: **C7-2**
Wednesday, June 13 - 3:50pm
135 GHz 98 mW 10 Gbps ASK Transmitter and Receiver Chipset in 40 nm CMOS, Naoko Ono, Mizuki Motoyoshi, Kyoya Takano, Kosuke Katayama, Ryuichi Fujimoto and Minoru Fujishima

Submission Number: **390**
Session/Paper Slot Number: **C22-2**
Friday, June 15 - 3:50pm
A 1.5GHz 1.35mW -112dBc/Hz In-band Noise Digital Phase-Locked Loop with 50fs/mV Supply-Noise Sensitivity, Amr Elshazly, Rajesh Inti, Mrunmay Talegaonkar and Pavan Kumar Hanumolu

Submission Number: **392**
Session/Paper Slot Number: **C7-1**
Wednesday, June 13 - 3:25pm
A 260 GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication, Jung-Dong Park, Shinwon Kang, Siva Thyagarajan, Elad Alon and Ali Niknejad

Submission Number: **393**
Session/Paper Slot Number: **C7-5**
Wednesday, June 13 - 5:05pm
A 94GHz mm-Wave to Baseband Pulsed-Radar for Imaging and Gesture Recognition, Amin Arbabian, Shinwon Kang, Steven Callender, Jun-Chau Chien, Bagher Afshar and Ali Niknejad

Submission Number: **395**
Session/Paper Slot Number: **C21-3**
Friday, June 15 - 2:20pm
A 900mA 93% Efficient 50µA Quiescent Current Fixed Frequency Hysteretic Buck Converter Using a Highly Digital Hybrid Voltage- and Current-mode Control, Qadeer Khan, Amr Elshazly, Sachin Rao, Rajesh Inti and Pavan Hanumolu

Submission Number: **396**
Session/Paper Slot Number: **J-C6-2**
Wednesday, June 13 - 3:50pm
A 3.14 um^2 4T-2MTJ-Cell Fully Parallel TCAM Based on Nonvolatile Logic-in-Memory Architecture, Shoun Matsunaga, Sadahiko Miura, Hiroaki Honjou, Keizo Kinoshita, Shoji Ikeda, Tetsuo Endoh, Hideo Ohno and Takahiro Hanyu