2013 Symposia on VLSI Circuits Short Course

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Abstract

For the past four decades, relentless focus on transistor scaling and Moore's Law led to ever-higher transistor performance and density, resulting in tremendous increases in functionality and performance. Historically, Moore's Law transistor scaling meant so-called "classic scaling" which was proposed by Dennard where gate oxide thickness, gate length and channel width were scaled by a constant factor in order to provide a delay improvement of at constant power density. As the transistor gate length and the gate oxide thickness scale down, physical limitations, such as off-state leakage current and power density, make geometric scaling an increasingly challenging task. The introduction of strain silicon technology and high-k + metal gate transistors broke through some of these scaling barriers. However, as dimensions are further reduced, there are a number of challenges to be overcome: capacitance, resistance, gate control, channel mobility, and variation. To continue historical trends of both area and performance improvement requires novel solutions. This short course will discuss historical transistor scaling trends, device scaling issues and potential future directions for continuing Moore's Law into the next decade.

Biography

Seok-Hee Lee received the B.S. and M.S. degrees in Materials Science and Engineering from Seoul National University, Seoul, Korea, in 1988 and 1990, respectively, and the Ph.D. degree in Materials Science and Engineering from Stanford University, Stanford, CA. in 2000. Since 2010, he has been with the faculty of the Department of EE in KAIST, Korea, as an Associate Professor. Since 2013, he is with S.K. Hynix as the President of Future Technology Research Center. His main interest is on nano-scale devices and fabrication. From 1990 to 1995, he was with the Advanced Semiconductor Development group, Hyundai Electronics (now Hynix Semiconductor), Korea, where he worked in the area of gate oxide scaling and reliability. In 1994, he discovered a new breakdown mechanism, quasi-breakdown (or soft-breakdown), in ultra-thin gate oxide regime. The research was reported at IEDM94 and has since developed into a new area of study in oxide reliability. From 2000 to 2010, he was with the Portland Technology Development group, Intel Corporation, Hillsboro, OR, where he worked on process integration and yield on Intel。ッs 130-, 90-, and 65-nm advanced CMOS logic technologies. Dr. Lee has received the Intel Achievement Award three times (Intel highest recognition for technical achievement) and 11 Intel Divisional Recognition Awards for his technical achievements in transistor and process development.

He was a committee member for CMOS devices and technology subcommittee for 2008-2009 IEDM, the chair for the same subcommittee in 2010 IEDM, and Asian arrangement chair for 2011 and 2012 IEDM. He is currently emerging technology chair for 2013 IEDM. He is also serving International Conference on Solid State Devices and Materials (SSDM) as a steering committee member of for 2011-2013 meetings.