2013 Symposia on VLSI Circuits Short Course

(Suzaku Ⅰ)

Tuesday, June 11

10:45-11:45 Impact of Technology on Digital Design

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Abstract

Mainstream digital design – with its underpinning on CMOS technology – has largely remained unchanged over multiple process nodes. However, fundamental shifts in device technology / characteristics have caused subtle but substantial changes in circuit design as designers have adapted and exploited them. This is most apparent in the area of SRAM memory designs incorporating memory bit-cells, digital logic and power collaterals. Using these building blocks as example cases we look at shifts in digital circuit design caused by technology innovations such as the advent of strained silicon and the incorporation of steep sub-threshold slope devices. The talk highlights that mature digital design has been in a constant state of evolution with the advent of new devices and the shift in emphasis from performance to power and energy.

Biography

Dinesh Somasekhar is a Senior Staff Scientist at Intel. He is currently responsible for the memory strategy on the high-performance-computing program under Intel Federal. He received the B.E. degree in Electronics Engineering from the Maharaja Sayajirao University Baroda, India, in 1989, the M.E degree in Electrical Communications Engineering from Indian Institute of Science Bangalore, India, in 1990, and the Ph.D. degree from Purdue University in West Lafayette in 1999. From 1991 to 1994 he was an I.C. Design Engineer at Texas Instruments, Bangalore, India, where he designed ASIC compiler memories and interface I.C.s. From 1999-2011 was with Circuits Research Lab, Intel R&D, Hillsboro, Oregon. From 2011-2012 he was with Global Foundries, Sunnyvale, CA. He has published 35 papers, 3 book chapters, and holds over 70 patents in the field of VLSI. Dr. Somasekhar served as Mentor at the Semiconductor Research Consortium, and has participated in the Technical Program Committee of ISLPED, ISQED, DATE, GLVLSI and CICC.