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13:40-14:40 3D Heterogeneous System Integration and New 3D LSIs

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Abstract

A new 3D heterogeneous system integration technology called a super-chip integration is described. A number of known good dies (KGDs) with different sizes and different devices are simultaneously aligned and bonded onto lower chips or wafer by a chip self-assembly method using the surface tension of liquid in the super-chip integration. Possibilities of new 3D LSIs by a super-chip integration such as 3D stacked multicore processor with self-test and self-repair function, GPU stacked 3D image sensor with extremely fast processing speed and 3D stacked reconfigurable processor with spin memory are discussed.

Biography

Mitsu Koyanagi received the Ph.D. degrees in electronic engineering from Tohoku University in 1974 and then joined the Central Research Laboratory, Hitachi Ltd. where he invented a stacked capacitor DRAM memory cell. In 1985, he joined the Xerox Palo Alto Research Center, California where he worked on research and development of sub-micron CMOS devices, poly-silicon thin film transistors and the design of analog/digital LSIs. In 1988 he joined Hiroshima University where he worked on sub-0.1um device, poly-Si TFT devices, 3-D integration technology, optical interconnection and parallel computer system specific for scientific computation. He proposed three-dimensional integration technology based on wafer-to-wafer bonding and Through-Si Via (TSV) for the first time in 1989. Since 1994, he has been a professor in Tohoku University where his current interests are 3-D integration technology, optical interconnection, nano-CMOS devices, memory devices, parallel computer system, retinal prosthesis chip and brain-machine interface. He was awarded the 2006 IEEE Jun-ichi Nishizawa Medal, the 1996 IEEE Cledo Brunetti Award, the National Medal with Purple Ribbon in Japan in 2011, and the Award of Ministry of Education, Culture, Sports, Science and Technology in 2001, and so on. He is an IEEE fellow.