2013 Symposia on VLSI Circuits Workship

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15:55-16:55 3-D Stacking, Solving the Interconnect Bandwidth / Power / Complexity Problem

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Abstract

In recent years, chip to chip communication has become the critical determinant of overall system performance. Despite SerDes rates doubling every four years, the resulting bandwidth increase falls far behind the demands of wireless communications, which sees bandwidth in air tripling every eighteen months. Increasing SerDes rates also come at the expense of I/O power and complexity, to a degree where I/O power is once again becoming a dominant concern in thermally constrained systems. 3-D stacking offers an order of magnitude reduction in inter-chip power/Gb/s over SerDes with vastly simplified design constraints. This talk will describe the implementation of a heterogeneous stacked device that uses a silicon interposer to connect 16x28Gb/s SerDes (450Gb/s in each direction) to an FPGA in a single package.

Biography

Liam Madden is corporate vice president of FPGA Development and Silicon Technology at Xilinx. He has responsibility for FPGA design, Advanced Packaging (including 3-D Chip Stacking) and Foundry Technology. Madden joined Xilinx in 2008, bringing more than 25 years experience in design and technology leadership positions. He has contributed to a range of industry leading products, including: high performance and low power microprocessors (Alpha and StrongArm at DEC), embedded processors and IP (MIPS) and consumer devices (Xbox 360 at Microsoft). He holds a BE degree from UCD and an M.Eng. degree from Cornell University.