

A 1GHz Power Efficient Single Chip Multiprocessor System for Broadband Networking Applications

Sribalan Santhanam, Randy Allmon, Krishna Anne, Randel Blake, Nils Bunger, Brian Campbell, Michael Carlson, Zongjian Chen, Jeff Cheng, Tuan Do, Dan Dobberpuhl, Joe Ingino, David Kidd, David Kruckemyer, Jong Lee, Dan Murray, Steve Nishimoto, Lief O'Donnell, Maksim Oyker, Mukaya Panich, Mark Pearce, Don Priore, Dan Rodriguez, Robert Rogenmoser, Dongwook Suh, Venkatesh Sundaresan, Erik Supnet, Vincent Von Kaenel, Gar Yee, George Yiu, Chinh Vo and Ricky Wen

Broadcom Corporation
San Jose, CA
USA

The Broadcom BCM12500 is a high performance System On a Chip (SOC) targeted at network centric tasks. The chip consists of two high performance SB-1 MIPS64 CPU's, a shared 512KB L2 cache, a DDR memory controller, three Ethernet MAC's and integrated I/O, including LDT™ high speed I/O and implements fully coherent memory transactions. The die measures 14.2mm by 13.3mm in a 0.15µm CMOS technology and has a power dissipation of 13W at 1.2V and 1GHz.