75 Word Abstract

A 512 Kbit low-voltage NV-SRAM with the size of a conventional SRAM

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This paper describes two new circuit techniques for nonvolatile SRAMs with back-up ferroelectric capacitors (NV SRAMs). These circuits are able to overcome the size and low-voltage-reliability problems faced by the original NV-SRAM. A new 0.25 μm NV-SRAM cell occupies 9.7 μm^2, that is the same area as an SRAM cell. A high-voltage/negative-voltage plate line driver allows a low voltage-operation NV-SRAM array's improving its nonvolatile retention characteristics. A 512-Kbit test macro has also been designed.