# Abstract

## A 800MHz Single Cycle Access 32entry Fully Associative TLB with 240ps Access Match Circuit

Masaya Sumita

Microprocessor Development Center,
Matsushita Electric Industrial Co.,Ltd.

Nagaokakyo, Kyoto, Japan

This paper describes a study of match circuits with content addressable memory (CAM). We proposed and studied two CAM match circuits; a differential current latch sense type and a cascade dynamic structure type (CDS-type). And then we developed a 32entry fully associative translation look-aside buffer (TLB) with CDS-type, using 0.13μm six level metal CMOS technology. The TLB enables 800MHz single cycle physical CACHE access. The power consumption is only 40mW at 1.5V and 800MHz operation.