Abstract

A Reconfigurable Multilevel Parallel Graphics Cache Memory with 75 GB/s Parallel Cache Replacement Bandwidth

Se-Jeong Park[1], Jeong-Su Kim, Ramchan Woo, Se-Joong Lee, Kang-Min Lee, Tae-Hum Yang[2], Jin-Yong Jung[2] and Hoi-Jun Yoo

Department of Electrical Engineering
Korea Advanced Institute of Science and Technology, Taejon, Korea

[2]Advanced Circuit Design Team, Memory R&D Division
HYUNDAI Electronics, Ichon, Korea

A dedicated single-chip multilevel parallel graphics cache memory for high-speed parallel texture mapping in PC graphics has been fabricated by a 0.16 μm DRAM technology. The proposed cache architecture is composed of four components; 1) an 8 MB DRAM L2 cache, 2) eight 16 KB SRAM L1 parallel caches, 3) eight pipelined texture data filters, 4) serial-to-parallel latches. It has a reconfigurable architecture and 75 GB/sec parallel L1 cache fill bandwidth by a hidden double data transfer scheme.

[1]e-mail : sjpark@core.kaist.ac.kr