A 0.13μm 6GHz 256x32b Leakage-tolerant Register File

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Abstract

This paper describes a 256x32b 4-read, 4-write ported register file for 6GHz operation in 1.2V, 0.13μm technology. The local bitline uses a pseudo-static leakage tolerant scheme to achieve 8% faster read performance and 36% higher DC noise robustness (with 6x active leakage reduction) compared to dual-Vt scheme optimized for high-performance.