75 Word Abstract

A Cell Ttransistor Scalable Array Architecture for High-Density DRAMs

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The limitation of cell transistror scaling due to stress-bias by high wordline voltage is a severe problem. In 0.13-um DRAM generation, the gate oxide thickness of cell transistor becomes twice larger than that of Logic LSIs. The proposed DRAM architecture reduces stress-bias to half by writing "1" and "0" data in different timing. This enables gate oxide thickness as thin as that of Logic LSIs, and reduces memory cell size to 87% in 0.13-um generation.