W/WN/Poly gate implementation for sub-130 nm vertical cell DRAM

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ABSTRACT

In this paper, we present the implementation of W/WN/poly gates in a 135 nm sub-8F2 vertical cell DRAM technology with dual gate oxide planar support transistors. Key features include low sheet resistance wordlines, high performance peripheral logic circuitry and a scalable memory cell array. A process flow detailing the decoupling of the array and support regions of the DRAM to achieve planar support transitors with Leff (nfet) < 140 nm is discussed.