A Manufacturable 25nm Planar MOSFET Technology

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ABSTRACT

We present here the results of study of manufacturability of sub-50nm MOSFET's using tools routinely available for production of 0.18 μm CMOS generation. We show that by adapting 248nm lithography, using non-equilibrium *n*-type junction formation and specially developed low-temperature processing one can manufacture devices with gate lengths as small as 15nm. It is also confirmed that heavily pocketed devices with sub-50nm gates show deterioration in performance suggesting that heavy pockets should be re-considered as the way to quench the short channel effects for sub-50nm generations in favor of, e.g., double-gated devices with low doping.