

## **High Performance sub-60 nm SOI MOSFETS with 1.2 nm Thick Nitride/Oxide Gate Dielectric**

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### **Abstract**

High performance sub-60nm SOI CMOS transistors have been developed. Aggressively scaled, 1.2 nm thick, gate dielectric sandwich containing silicon nitride and dioxide layers allowed full control of boron penetration with manageable level of gate leakage. Excellent values of  $I_{dsat}$  of  $850 \mu A/\mu m$  and  $500 \mu A/\mu m$  for NMOS and PMOS were respectively obtained at  $V_{dd}=1.2$  V and  $I_{off}=100$  nA/ $\mu m$ . CV/I metric was 1.0 and 1.9 ps for NMOS and PMOS respectively.