

Impact of CMOS process scaling and SOI on the soft error rates of logic processes

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Abstract

Technology scaling, a reduction in operating voltages, and the increase in cache size and circuit complexity have been key enablers to achieving the performance improvement expectation dictated by Moore's Law. The resulting reduction in the node charge of circuit latches and cache cells has resulted in an ever increasing soft error rate (SER) estimation for logic components. This paper will report the SER impact of process scaling over four technology generations (0.35, 0.25, 0.18, 0.13 μm) and provide an experimental assessment of alpha and, for the first time, neutron SER on advanced SOI processes, which have been considered as a possible method to reduce the SER of advanced technologies.