A Robust Array Architecture for a Capacitorless MISS Tunnel-Diode Memory

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With the aim of applying a MISS tunnel-diode cell to a high-density RAM, we studied its problems and developed three circuit techniques to solve them. The first, a hierarchical bit-line structure reduces the number of sense amplifiers. The second, a twin-dummy-cell technique generates a proper reference signal. The third, a standby-voltage control scheme suppresses the degeneration of the signal current. These techniques enable the capacitorless MISS-diode memory cell, whose effective cell area is $6F^2$.