Threshold-voltage Balance for Minimum Supply Operation

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The difference between the threshold voltages (V_t) of PMOS and NMOS transistor is a critical issue in the operation of low voltage circuits. The P/N V_t balancing profit is analyzed in terms of sub-threshold leakage current, minimum supply voltage, and static noise margin. Balancing the P/N V_t reduces the lowest required supply voltage by 0.15-0.3 V. The use of our proposed V_t matching scheme enables CMOS LSI minimum supply voltage processing at 0.1 V.