Crosstalk Delay Analysis of a 0.13-µm-node Test Chip and Precise Gate-level Simulation Technology

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The impact of crosstalk on delay was examined by measuring a 0.13-µm-node test chip. This examination revealed three requirements for precise gate-level simulation technology: consideration of degradation change dependent on relative-signal-arrival-time, static-timing-analysis based operation, and quantitative estimation of the degradation accumulation caused by multiple aggressors. A candidate for this simulation technology is evaluated, and maximum error between the measured and simulated degradations was reduced to less than one sixth of that with a conventional method.