

Design & Validation of the Pentium® III and Pentium® 4 Processors Power Delivery

Tawfik Raha-Arabi, Greg Taylor, Matthew Ma, and Clair Webb

Intel Corporation / Logic Technology Development

5200 NE ElamYoung Parkway

Hillsboro, Oregon, 97124

Email: Tawfik.r.Arabi@intel.com

In this paper, we present an empirical approach for the validation of the power supply impedance model. The model is widely used to design the power delivery for high performance systems. For this purpose, several silicon wafers of the Pentium® III and Pentium® 4 processors were built with various amount of decoupling. The measured data showed significant discrepancies with the model predictions and provided useful insights in investigating the model regions of validity.