

A 6GHz, 16Kbytes L1 Cache in a 100nm Dual-V_T Technology Using a Bitline Leakage Reduction (BLR) Technique

Yibin Ye, Muhammad Khellah, Dinesh Somasekhar, Ali Farhang and Vivek De
Microprocessor Research, Intel Labs, Hillsboro, OR, USA

A L1 cache testchip with dual-V_T cell and a bitline leakage reduction (BLR) technique has been implemented in a 100nm dual-V_T technology. Area of a 2KBytes array is 263μm X 204μm, which is virtually the same as the best conventional design with high-V_T cell. BLR eliminates impacts of bitline leakage on performance and noise margin with minimal area overhead. Bitline delay improves by 23%, thus enabling 6GHz operation. Energy consumption per cycle is 15% higher.