Supply Voltage Strategies for Minimizing the Power of CMOS Processors

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Abstract

This paper presents a dual supply voltage strategy for reduction of the total (static and dynamic) power of high performance CMOS processors. An optimization procedure that takes the circuit activity factor into account is performed to find the power supply and threshold voltage for minimum total power at given performance levels. It is shown that 50% power reduction without performance loss is attainable by adopting a low supply voltage (0.5V) for high activity circuits in addition to the nominal supply voltage (1.2V) for low activity circuits in a 100nm node CMOS technology.