Highly Manufacturable 32Mb ULP-SRAM Technology by using Dual Gate Process for 1.5V Vcc Operation

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For 1.5V low Vcc operation and high performance full-CMOS low power SRAM using dual gate and Co salicide technology was developed. We evaluated the new technology includes i)0.11um fine patterning implemented by phase shift mask(PSM) and optical proximity correction(OPC), ii)dual gate CMOS transistor with thin gate oxide, iii)improvement of Co salicide process to minimize the leakage current. These results enable to achieve 32Mb high density 6T LP SRAM cell.