Femto-Second CMOS Technology with High-k Offset Spacer and SiN Gate Dielectric with Oxygen-enriched Interface

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We demonstrate 40-nm CMOS transistors for the 70-nm technology node. This transistor uses a high-k offset spacer in achieving both a short-channel and high drivability along with SiN gate dielectrics with oxygen-enriched interface to suppress both the gate-leakage current and boron penetration. N-MOSFET and P-MOSFET have high drive currents of 0.68 and 0.30 mA/μm with I_{off} = 10 nA/μm. The record gate delay of 280 fs (3.6 THz), for an N-MOSFET with the gate length of 19 nm, has also been achieved.