Fully-Depleted-Collector Polysilicon-Emitter SiGe-Base Vertical Bipolar Transistor on SOI

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Abstract

A novel vertical bipolar transistor on SOI is proposed and demonstrated. The SOI silicon layer thickness is comparable to that used in SOI CMOS, and no subcollector layer or deep trench isolation are required. Simulated device characteristics are shown. The transistor is demonstrated in a polysilicon-emitter SiGe-base npn implementation on SOI with a 140-nm silicon layer. The fabricated npn bipolar transistors exhibit a BVceo of 4.2V and a peak f_T of over 60GHz.