A Strategy using a Copper/low-k BEOL Process to prevent Negative-Bias Temperature Instability (NBTI) in p-MOSFETs with Ultra-Thin Gate Oxide

A. Suzuki, K. Tabuchi, H. Kimura, T. Hasegawa, S. Kadomura,
LSI Technology Development Group, S.N.C, Sony Corporation 4-14-1, Asahi, Atsugi, Kanagawa, 243-0014, Japan
Tel:+81-462-30-5508, Fax:+81-462-30-6556, E-mail: AtsushiC.Suzuki@jp.sony.com

K. Kakamu*, H. Kudo**, M. Kawano**, A Tsukune** and M. Yamada**
* VLSI Laboratory, Fujitsu VLSI Ltd., 1500 Mizono, Tado-cho, Kuwana-gun, Mie-ken, 511-0192, Japan
** Advanced Devices, Process Integration Dept. Manufacturing Technol. Develop. Div., Fujitsu Ltd., 1500 Mizono, Tado-cho, Kuwana-gun, Mie-ken, 511-0192, Japan

This paper is a report on the effect of processing to form copper/low-k interconnects on the NBTI. We found that the NBT-stress lifetime of copper/low-k interconnects is shorter than that of aluminum/SiO_2 interconnects. The NBTI strongly depends on the cap layer over the copper/low-k, on the intermetal dielectric film, on the barrier-metal film, and on the temperature of post-metal annealing. Based on these results, we developed methods for reducing the NBTI in next-generation MOSFETs.