Advanced Cu/Low-k (k = 2.2) Multilevel Interconnect for 0.10/0.07μm Generation

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A spin-on dielectric (SOD, k=2.2) has been integrated with Cu for 0.10/0.07μm generation. To minimize interconnect capacitance, conventional CVD cap layer (k=4.5–7.5) is replaced by a SOD dielectric (k=2.9) and no stop layer for trench etch is used for the porous inter-metal dielectric (IMD). The issue of photoresist poisoning is resolved by nitrogen-free IMD processing. Using polymeric abrasive together with polishing parameters designed in a low friction domain for planarization, 6-level Cu/porous SOD multilevel interconnect is demonstrated for the first time. Electrical testing shows promising results for the high-performance dual-damascene structure.