Integration of High Performance Dual Workfunction Logic CMOS Transistors with a Dense $8F^2$ Vertical DRAM Cell

Rajesh Rengarajan[*], Rajeev Malik[*], Haining Yang[#], Wendy Yan[#], Ravikumar Ramachandran[*],

Boyong He[#], Rama Divakaruni[#], Yujun Li[#]

[*]Infineon Technologies and [#]IBM Microelectronics

IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533, USA

e-mail: rajesh.rengarajan@infineon.com

Abstract

In this paper, we report on integration of high performance dual workfunction logic CMOS transistors with a commodity $8F^2$ vertical DRAM cell for high performance stand-alone DRAM and low-cost low-power embedded DRAM applications. Key process integration features that exploit novel aspects of the vertical DRAM cell to enable a high performance cost-effective embedded DRAM technology are presented. The impact of pre-metal-dielectric reflow thermal budget on dual workfunction CMOS device characteristics is discussed.