Title:

UX6-100 nm Generation CMOS Integration Technology with Cu / Low-k Interconnect

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Abstract:

UX6-100 nm generation CMOS integration technology is demonstrated. Various transistor performances (UHP, HP, MP, Over-drive), yields of unit processes and 6T-SRAM operation were verified using full-integration processed wafers. To meet the requirement for various performance, multi-V_{TH}, multi-thickness gate-oxide process, low-leakage gate dielectric are incorporated in FEOL. To suppress RC increase compared to previous generation, low-k (Keff=3.1) interlayer dielectric and Cu interconnect dual damascene are incorporated in BEOL.