Poly-Si Gate CMOSFETs with HfO_2-Al_2O_3 Laminate Gate Dielectric for Low Power Applications

Jong-Ho Lee, Yun-Seok Kim, Hyung-Seok Jung, Jung-Hyoung Lee, Nae-In Lee, Ho-Kyu Kang, Ja-Hum Ku, Hee Sung Kang, Youn-Keun Kim, Kyung-Hwan Cho, and Kwang-Pyuk Suh

Advanced Process Development Project, System LSI Business, Samsung Electronics Co., Ltd.
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do, Korea, 449-711

Phone: 82-31-209-6350, Fax: 82-31-209-6299, E-mail: knight97@samsung.co.kr

For the first time, we have integrated poly-Si gate CMOSFETs with HfO_2-Al_2O_3 laminate gate dielectric (EOT=14.6Å) grown by Atomic Layer Deposition (ALD). The gate leakage currents are 3.7μA/cm^2 (Vg=+1.0V) for nMOSFET and 0.2μA/cm^2 (Vg=-1.0V) for pMOSFET. The fixed charge is decreased using HfO_2-Al_2O_3 laminate gate dielectric. Ion vs. Ioff plots of planar CMOS transistor with high-k is shown for the first time in this paper. The measured saturation currents at 1.2V Vdd are 430μA/μm (Ioff=10nA/μm) for nMOSFET and 160μA/μm (Ioff=10nA/μm) for pMOSFET.